

Edition (12/2012)

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We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly. Necessary corrections are included in subsequent editions. Suggestions for improvement are welcomed.

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Preface

Contents of this Manual

- ❑ Detailed description of the individual function groups of the EB 200P
- ❑ Connector pin assignment and jumper assignment

Target Audience of this Manual

This manual is intended for hardware developers who want to use the ERTEC 200P for new products. Experience working with processors and designing embedded systems and knowledge of Ethernet are required for this.

The manual serves as a reference for software developers. Sections 7 and 8 describe the jumper settings and connectors that are required for software tests (e.g. debugging, terminal outputs, etc.).

Structure of this Manual

This manual describes the ERTEC 200P evaluation board. The manual is structured as follows:

- Section 1 Introduction
- Section 2 Hardware Structure of the EB 200P
- Section 3 Memory Distribution of the EB 200P
- Section 4 Operating Modes of the EB 200P
- Section 5 JTAG Interface of the EB 200P
- Section 6 Settings of the EB 200P
- Section 7 Connectors of the EB 200P
- Section 8 Jumpers of the EB 200P
- Section 9 Mechanical Structure of the EB 200P
- Section 10 List of Terms and References

When working with modules, always take precautionary measures against electrostatic charge (ESD – Electrostatic Sensitive Devices).

For module handling and installation, refer to /1/.

This manual will be updated as required. You can find the current version of the manual on the Internet at <http://comdec>.

Guide

To help you quickly find the information you need, this manual contains the following aids:

- A complete table of contents as well as a list of all figures and tables in the manual are provided at the beginning of the manual.
- A glossary containing definitions of important terms used in the manual is located following the appendices.
- References to other documents are indicated by the document reference number enclosed in slashes (/No./). The complete title of the document can be obtained from the list of references at the end of the manual.

Additional Support

If you have questions regarding use of the described block that are not addressed in the documentation, please contact your Siemens representative.

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1 **Introduction**

This manual describes the procedure for using the ERTEC 200P for HW development of a PROFINET IO device and the properties of the EB 200P evaluation board.

The intended use of the EB 200P evaluation board is as follows:

- It serves as a template for development of your own PROFINET IO device hardware.
- It supports development and testing of your own PROFINET IO device application software.
- It enables testing of your hardware on a supplementary board together with the EB 200P, where applicable.

1.1 **Procedure when using ERTEC 200P to develop your own PROFINET IO Device**

If you are using the recommended minimum configuration for a PROFINET IO device, no changes (or only minor changes) have to be made in the board support package (BSP) for your additionally required hardware. The board support package adapts the operating system to the hardware.

Procedure

You can use ERTEC 200P to develop your own hardware in one of two ways:

- By using a test board on the EB 200P to adapt and test your application circuit
- By using ERTEC 200P directly to develop and test your complete target hardware

Note the following boundary conditions for hardware development:

Debug interfaces for commissioning and testing

Always make provision for connectors on your hardware to the JTAG interface and, if possible, to a USB virtual serial interface (UART) of the ERTEC 200P in order to facilitate commissioning.

1.2 Structure of the EB 200P

The EB 200P is implemented in the form of a half-size PCI Express card. The PCI Express interface is used only for PC mode. In standard configuration the EB 200P is operated as a stand-alone module. The EB 200P is **supplied** by means of an external plug-in power supply (part of the development kit). For software debugging a JTAG interface is available, for more information about JTAG interface is in Chapter 5.

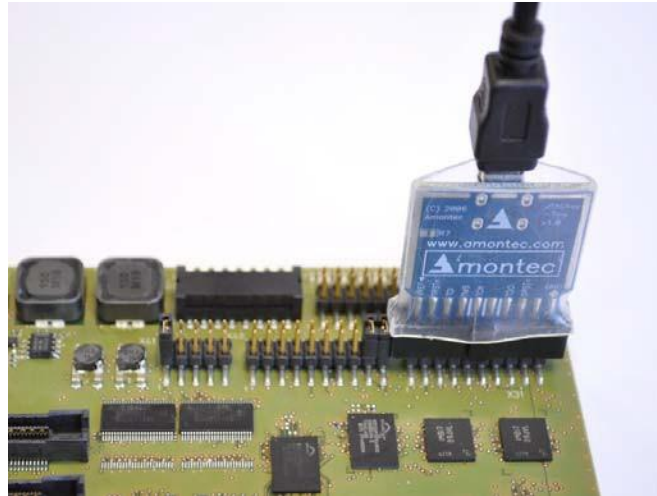


Figure 1: EB 200P with connected debugger

1.3 Features of the EB 200P

In addition to the ERTEC 200P with its integrated function groups, the following elements are available on the EB 200P:

- PC front panel element with
 - 2 RJ45 PROFINET sockets with integrated magnetics, with POF assembly option
 - 2 RJ45 TAP sockets for debugging purposes during development for MDI port
 - 2 LEDs **Link** and **Activity** per RJ45 socket
 - 4 LEDs for additional status indicators
 - BNC connector for PLL Sync signal
- Flash memory 32 Mbytes, Burst Mode, 2 chips 1Mx16bit in parallel
- SDRAM 128 Mbytes, 2chips 32Mx16bit in parallel
- I2C EEPROM
- SPI temperature sensor
- Debug and trace interface for ARM926EJ-S Microcontroller
- USB Virtual serial interface for monitoring
- Configuration and boot modes can be set via jumpers
- Various operating modes of the EB 200P can be set via jumpers
- Various connectors for external wiring

1.4 Block Diagram of the EB 200P

Blockdiagramm EB200P

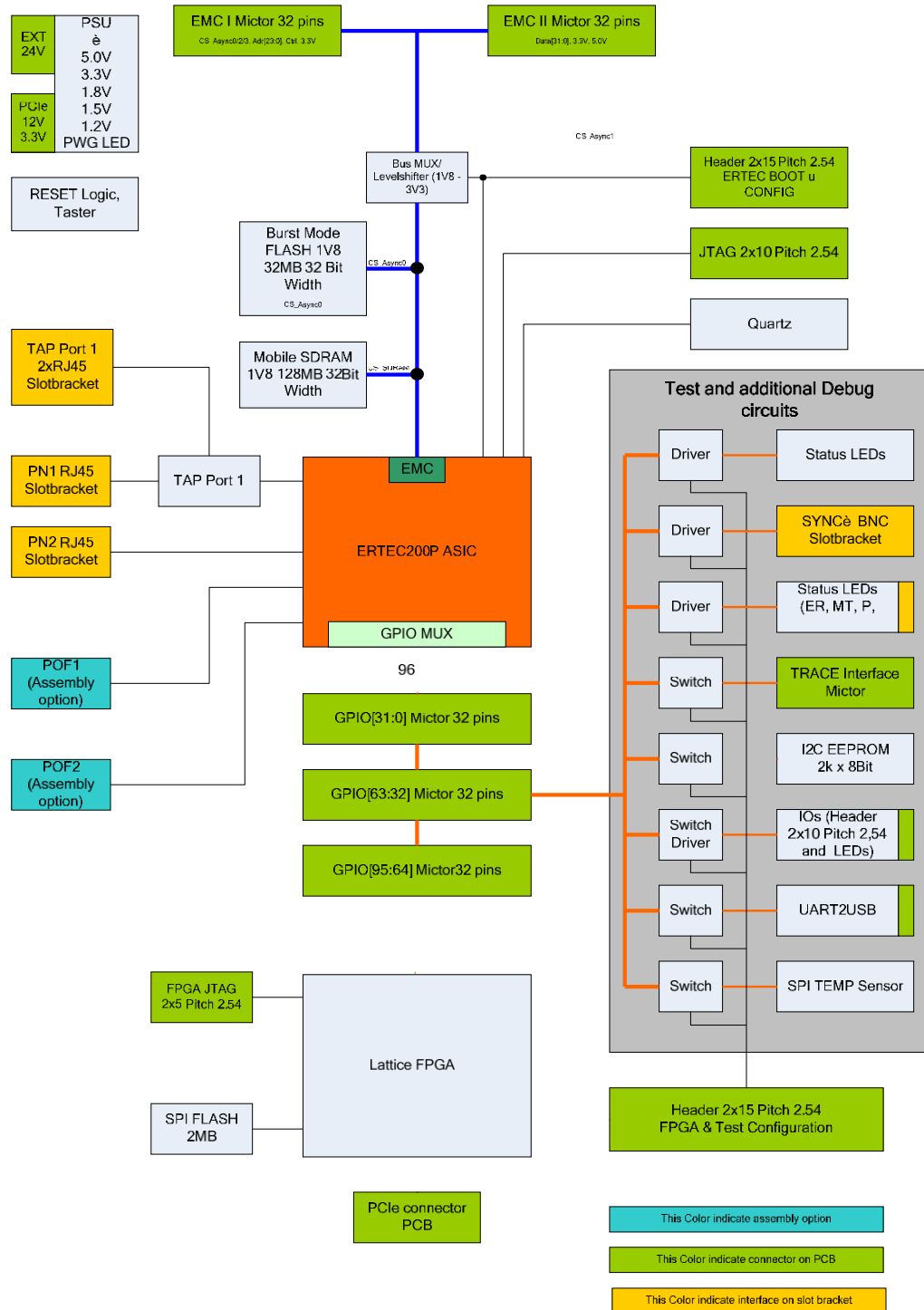


Figure 2: Block diagram of EB 200P

2 Hardware Structure of the EB 200P

2.1 ERTEC 200P

2.1.1 Function Overview

Refer to documents /1/ and /2/ for a detailed function description of the ERTEC 200P.

In this manual, only the main components are described briefly and represented in a block diagram.

The following four AHB masters are integrated in the ERTEC 200P:

- ARM926EJ-S with trace/debug port and high-performance interrupt controllers
- PNIP with 64 Kbytes of K-RAM for real-time Ethernet communication
- External host processor on the XHIF interface
- 32-channel DMA controller

The following I/O blocks are available to the masters:

- External memory controller (EMC) with SDRAM and SRAM controller
- Two Ethernet interfaces with integrated MII PHYs
- Blocks connected to APB bus
 - 96-bit GPIO
 - 4x UART
 - 2x SPI
 - 3x I²C
 - 6 timers
 - F-timer
 - 2x Watchdog
 - Boot ROM
 - System Control
 - Peripherie Interface
 - I-Filter

The multi-layer AHB bus system enables a largely independent operation of the masters. Internal arbitration logic prevents access conflicts if multiple masters want to access the same I/O block. The function groups of the ERTEC 200P are shown in block diagram. For block diagram please refer to /1/

2.1.2 Operating Modes of the EB 200P

Various configurations on the EB 200P can be set by means of jumpers X40.9/10 and X41.1/2. These jumpers are described in Section 7. The following configuration settings are possible on the ERTEC 200P.

Boot configuration	Cfg(6)	Cfg(5)	Cfg(4)	Cfg(3)	Cfg(2)	Cfg(1)	Cfg(0)
REF_CLK Tristate	x	x	x	x	x	x	Open
REF_CLK Output (25MHz)	x	x	x	x	x	x	Close
ARM Clock 125MHz	x	x	x	x	x	Close	x
ARM Clock 250MHz	x	x	x	x	x	Open	x
PLL Bypass on (Config(1) = Close)	x	x	x	x	Close	x	x
PLL Bypass off	x	x	x	x	Open	x	x
XHIF=16bit, XHIF_XWR = R/W	Close	Open	x	Close	x	x	x
XHIF=16bit, XHIF_XWR, XHIF_XWR separated	Close	Open	x	Open	x	x	x
XHIF=16bit, XHIF_XRDY active high	Close	Open	Open	x	x	x	x
XHIF=16bit, XHIF_XRDY active low	Close	Open	Close	x	x	x	x
XHIF=32bit, XHIF_XWR = R/W	Close	Close	x	Close	x	x	x
XHIF=32bit, XHIF_XWR, XHIF_XWR separated	Close	Close	x	Open	x	x	x
XHIF=32bit, XHIF_XRDY active high	Close	Close	Open	x	x	x	x
XHIF=32bit, XHIF_XRDY active low	Close	Close	Close	x	x	x	x
XHIF=off	Open	Open	Open	Open	x	x	x
XHIF=off, ARM926 Trace Port on	Open	Close	Close	Close	x	x	x
XHIF=off	Remaining combinations				x	x	x

Table 1 Selection of Operating Modes and System Functions for EB 200P

- XHIF mode: Cfg(6) jumper closed
The XHIF interface is active for access of a host processor system to internal components of the ERTEC 200P.
- Trace mode: Cfg(6) open, Cfg(5) close, Cfg(4) close, Cfg(3) close
The trace port is available to the user in this mode.

Following table shows configuration jumpers for test and debugging. Pin headers are labeled X42 and X43.

Function	Signal	Pin	Pin	Signal	Function when jumper is installed
Sync(0)	BNC tip pin	1	2	ERTEC GPIO(9)	Sync BNC Input
Sync(1)	BNC tip pin	3	4	ERTEC GPIO(0)	Sync BNC Output
Trace	Trace CS bus switch OE	5	6	GND	Trace Disabled
EEPROM	EEPROM CS bus switch OE	7	8	GND	EEPROM Enabled
User GPIOs	User GPIOs CS bus switch OE	9	10	GND	GPIOs Enabled
UART	UART CS bus switch OE	11	12	GND	UART Enabled
TEMP	TEMP CS bus switch OE	13	14	GND	SPI Sensor Enabled
F_XHIF(0)	FPGA_CONFIG(0)	15	16	GND	Same functionality as Cfg(3)-Cfg(6)
F_XHIF(1)	FPGA_CONFIG(1)	17	18	3.3V	
F_XHIF(2)	FPGA_CONFIG(2)	19	20	3.3V	
F_XHIF(3)	FPGA_CONFIG(3)	21	22	GND	
None	NC	23	24	NC	
None	NC	25	26	NC	
None	NC	27	28	NC	
None	NC	29	30	NC	

Table 2 Test and debug jumpers configuration

2.1.3 Boot Modes of the EB 200P

Various boot modes on the EB 200P can be set by means of jumpers X40.1/2 to X40.7/8.

The following boot modes are supported:

Boot source	Boot(3)	Boot(2)	Boot(1)	Boot(0)
NOR Flash (8bit)	Open	Open	Close	Open
NOR Flash (16bit)	Open	Open	Close	Close
NOR Flash (32bit)	Open	Open	Open	Open
XHIF	Open	Close	Open	Close

Table 3 Boot mode selection for EB200P

2.1.4 ERTEC 200P Processor and I/O

The ARM926EJ-S processor with interrupt controller is integrated in the ERTEC 200P. The processor and various standard I/O are available to users for their applications. These include the following function groups:

- ARM926EJ-S processors with
 - 125/250 MHz operating frequency that can be set via jumpers (see Operating Modes 2.1.2)
 - 16 Kbytes of instruction cache
 - 16 Kbytes of data cache
 - 256 Kbytes of data TCM
 - JTAG interface for debug interface
- Interrupt controller for asynchronous events (96 IRQ and 8 FIQ inputs)
- SDRAM controller 125 MHz/max. 256 Mbytes of address space (16/32-bit data width can be assigned)
- SRAM controller, up to 4 x 16 Mbytes (8/16/32-bit data width and timing can be assigned separately for all 4 areas)
- 2x Watchdog timer unit for monitoring module functions
- Timer unit for generating periodic trigger pulses
- F-timer for fail-safe applications
- GPIO ports for activating LEDs, etc.
- SPI interface for connecting serial EEPROM/Flash
- 4x UART

- 3x I2C

2.1.5 PNIP

The PNIP provides the required function for PROFINET IO. It contains the following functions:

- Configuration register for PNIP
- 64 Kbytes of K-RAM for RT and IRT communication

2.1.6 External Memory Controller (EMC)

EMC comprises of 2 different controllers, one supporting the SDRAM Memory devices (including Mobile SDRAM), the other supporting asynchronous SRAM timing in different flavors, including Burst Flash ROM memory devices.

SDRAM-Controller features:

- 16/32 Bit databus width
- PC133 SDRAM-compatible (125 MHz synchron is used in ERTEC 200P)
- 1 Bank with max. 256 MByte SDRAM (32 Bit databus)
- SDRAM support for following parts:
 - CAS-Latency: 2 or 3 clocks
 - Bank-address bits (1/2/4 internal banks), realized via the lowest two bits of the address bus MA(1:0)
 - 8/9/10/11 bits column-address MA(13), MA(11:2)
 - max. 14 bits row-address MA(15:2)

Asynchronous Controller features:

- Can be set to 8/16/32-bit data bus width (for each chip select programmable) chip selects
- The timing for each chip select can be set individually
- The response to ready signal can be set individually for each chip select
- The default setting is slow timing for booting purposes
- A maximum of 64 MB address area for each chip select
- Acknowledgement delay monitoring for external components can be set by software

The boot medium is always expected on chip select signal **XCS_PER0**. EB 200P board is equipped with Burst Mode FLASH connected to this CS signal. If extension board is used, one can reconnect chip select signals from the default state to extension board by changing of resistors. The following blocks of the EB 200P can be selected with the chip-select lines:

Chip Select	I/O	Function
XCS_PER0	Boot Flash / FLASH	2x 8Mbit x 16
XCS_PER1	reserved	8kbit x 32
XCS_PER2	extension board	16Mbit x 32
XCS_PER3	extension board	16Mbit x 32

Table 4 CS Areas of the EB 200P

2.1.7 Debug and Trace Interface

The ETM macro cell of the ARM926EJ-S can be used as a debug and trace interface in the ERTEC 200P. With this interface, the user software running on the ARM926EJ-S and the user data can be analyzed and traced. The ETM module is a standard module recommended by ARM on which various available debuggers can be run. If the trace interface is used, the XHIF interface is not available (configuration setting "Trace On", see Section 2.1.2). If the trace interface is used, the required parameter assignment of the ETM macro cell must be performed with the debugger, so that the required pins are switched to trace functionality.

For debug and trace functionality 38pin MICTOR connector is assembled on EB 200P. JTAG pins on MICTOR are directly connected to JTAG interface on ERTEC 200P. Signals for tracing can be connected or disconnected to/from ERTEC 200P GPIOs by bidirectional bus switch

The ETM macro cell is described in documents /9/ and /10/.

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