5G LDPC Intel® FPGA IP User Guide

Updated for Quartus® Prime Design Suite: **24.1**

IP Version: **21.1.5**

Online Version
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UG-20057

683107
2024.04.01

Contents

1. About the 5G LDPC Intel® FPGA IP

Low-density parity-check (LDPC) codes are linear error correcting codes that help you to transmit and receive messages over noisy channels. The 5G LDPC Intel® FPGA IP implements LDPC codes compliant with the 3rd Generation Partnership Project (3GPP) 5G specification for integration in your wireless design.

LDPC codes replace Turbo codes, popular in 3G and 4G wireless cellular communications. LDPC codes offer better spectral efficiency and support the high throughput for 5G new radio (NR).

Related Information

- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Creating Version-Independent IP and Qsys Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.
- 3GPP New Radio Specification
  The final equivalents are Release 15, 3GPP Technical Specification Group RAN 1, NR:
  - (1) Multiplexing and channel coding, 3GPP TS 38.212 (v15.3.0)
  - (2) Physical layer procedures for data, 3GPP TS 38.214 (v15.3.0)

1.1. 5G LDPC Intel FPGA IP Features

The 5G LDPC IP offers the following features:

- 3GPP 5G LDPC specification compliant
- For the decoder:
  - Improved block error rate (BLER) performance
  - Improved power efficiency of IP
  - Per-block modifiable code block length, code rate, base graph, and maximum number of iterations
  - Configurable input precision
  - Layered decoder scheduling architecture to double the speed of convergence compared to non-layered architecture
  - Early termination based on syndrome check on each iteration
  - Single or dual decoders
- For the encoder: per-block modifiable code block length and code rate
- No external memory requirement
- MATLAB and C++ models for performance simulation and RTL test vector generation
- Verilog HDL testbench option
- Avalon®streaming input and output interfaces

Related Information

- 3GPP New Radio LDPC Specification
- Avalon Streaming Interface Specifications

1.2. 5G LDPC Intel FPGA IP Device Family Support

The IP supports the following devices families:

- Agilex™ 5 devices
- Agilex 7devices
- Arria® 10 devices
- Stratix® 10 devices

For the device support levels for Intel FPGA IP, refer to *Device Support and Pin-Out Status* in the latest version of the *Intel Quartus Prime Pro Edition: Software and Device Support Release Notes*.

Related Information

Device Support and Pin-Out Status

1.3. 5G LDPC IP Release Information

Table 1. Release Information

Item	Description
Version	21.1.4
Release Date	August 2023
Ordering Code	IP-5G-LDPC

Intel verifies that the current version of the Quartus® Prime software compiles the previous public version of each IP. Intel does not verify that the Quartus Prime software compiles IP versions older than the previous version. The *Intel FPGA IP Release Notes* lists any exceptions.

Related Information

Intel FPGA IP Release Notes

1.4. 5G LDPC IP Performance and Resource Utilization

Intel generated the resource utilization and performance for the encoder and the decoder by compiling the designs with Intel Quartus Prime software v21.1 (23.2.1 for Agilex 5 devices). Only use these approximate results for early estimation of FPGA resources (e.g. adaptive logic modules (ALMs)) that a project requires.

Decoder

Table 2. Resource Utilization and Maximum Frequency for Agilex 5 Devices

Targeting A5EC065BB32AE5SR0 device. The f_{MAX} is the five-seeds average f_{MAX} reduced 15% for margins.

IN_WIDTH	NUM_DECODER	MAX_LF_DECODER0	MAX_LF_DECODER1	ALMs	M20K Memory Blocks	f_{MAX} (MHz)
6	1	384	-	53,980	762	298

Table 3. Resource Utilization and Maximum Frequency for Agilex 7 Devices

Targeting AGFB014R24B2I2V device. The f_{MAX} is the five-seeds average f_{MAX} reduced 15% for margins.

IN_WIDTH	NUM_DECODER	MAX_LF_DECODER0	MAX_LF_DECODER1	ALMs	M20K Memory Blocks	f_{MAX} (MHz)
6	1	384	-	58,720	762	548
6	1	192	-	30,082	402	572
6	1	128	-	19,898	281	574
6	1	96	-	15,604	221	574
6	2	-	192	88,696	1165	556
6	2	-	128	78,828	1044	549
6	2	-	96	74,520	984	550
5	1	384	-	53,588	677	561
5	1	192	-	27,420	367	572
5	1	128	-	18,314	258	577

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IN_WIDTH	NUM_DECODER	MAX_LF_DECODER0	MAX_LF_DECODER1	ALMs	M20K Memory Blocks	f_{MAX} (MHz)
5	1	96	-	14,134	203	576
5	2	-	192	80,494	1045	555
5	2	-	128	71,751	936	541
5	2	-	96	67,565	881	547

Table 4. Resource Utilization and Maximum Frequency for Arria 10 Devices

Targeting 10AT115S1F45E1SG device. The f_{MAX} is the five-seeds average f_{MAX} reduced 15% for margins.

IN_WIDTH	NUM_DECODER	MAX_LF_DECODER0	MAX_LF_DECODER1	ALMs	M20K Memory Blocks	f_{MAX} (MHz)
6	1	384	-	47,261	762	306
6	1	192	-	24,698	402	339
6	1	128	-	17,015	281	348
6	1	96	-	13,381	221	360
6	2	-	192	72,690	1165	290
6	2	-	128	64,925	1044	294
6	2	-	96	61,238	984	296
5	1	384	-	41,906	677	312
5	1	192	-	21,654	367	339
5	1	128	-	15,036	258	353
5	1	96	-	11,842	203	353
5	2	-	192	63,292	1045	305
5	2	-	128	56,714	936	313
5	2	-	96	53,658	881	318

Table 5. Resource Utilization and Maximum Frequency for Stratix 10 Devices

Targeting 1SG280HU2F50E2VG device. The f_{MAX} is the five-seeds average f_{MAX} reduced 15% for margins.

IN_WIDTH	NUM_DECODER	MAX_LF_DECODER0	MAX_LF_DECODER1	ALMs	M20K Memory Blocks	f_{MAX} (MHz)
6	1	384	-	62,090	762	384
6	1	192	-	31,889	402	413
6	1	128	-	21,772	281	409
6	1	96	-	16,838	221	419
6	2	-	192	93,439	1165	365
6	2	-	128	83,526	1044	365
6	2	-	96	79,157	984	374
5	1	384	-	56,806	677	369
5	1	192	-	29,469	367	412
5	1	128	-	20,063	258	411

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IN_WIDTH	NUM_DECODER	MAX_LF_DECODER0	MAX_LF_DECODER1	ALMs	M20K Memory Blocks	f_{MAX} (MHz)
5	1	96	-	15,690	203	433
5	2	-	192	84,685	1045	378
5	2	-	128	75,905	936	383
5	2	-	96	71,549	881	373

Table 6. Resource Utilization and Maximum Frequency for Stratix 10-L Devices

Targeting 1SG280HU2F50E2LG device. The f_{MAX} is the five-seeds average f_{MAX} reduced 15% for margins.

IN_WIDTH	NUM_DECODER	MAX_LF_DECODER0	MAX_LF_DECODER1	ALMs	M20K Memory Blocks	f_{MAX} (MHz)
6	1	384	-	62,297	762	379
6	1	192	-	31,849	402	394
6	1	128	-	21,715	281	403
6	1	96	-	16,812	221	405
6	2	-	192	93,144	1165	359
6	2	-	128	83,298	1044	360
6	2	-	96	78,968	984	368
5	1	384	-	56,768	677	378
5	1	192	-	28,754	367	403
5	1	128	-	20,038	258	401
5	1	96	-	15,684	203	399
5	2	-	192	85,326	1045	367
5	2	-	128	76,386	936	381
5	2	-	96	71,937	881	367

Encoder

Intel generated the data for the following devices:

- Intel Agilex 5 A5EC065BB32AE5SR0
- Agilex 7 AGFA014R24A2E2VR0
- Intel Arria 10 10AT115S1F45E1SG
- Intel Stratix 10 1SG280HU2F50E2VG
- Intel Stratix 10-L 1SG280HU2F50E2LG

Table 7. Resource Utilization and Maximum Frequency

The f_{MAX} is the five-seeds average f_{MAX} reduced 15% for margins.

Device	ALMs	M20K Memory Blocks	f_{MAX} (MHz)
A5EC065BB32AE5SR0	17,040	23	400
AGFA014R24A2E2VR0	17,684	23	554

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