LM25119/LM25119Q Wide Input Range Dual Synchronous Buck Controller

Check for Samples: LM25119/25119Q

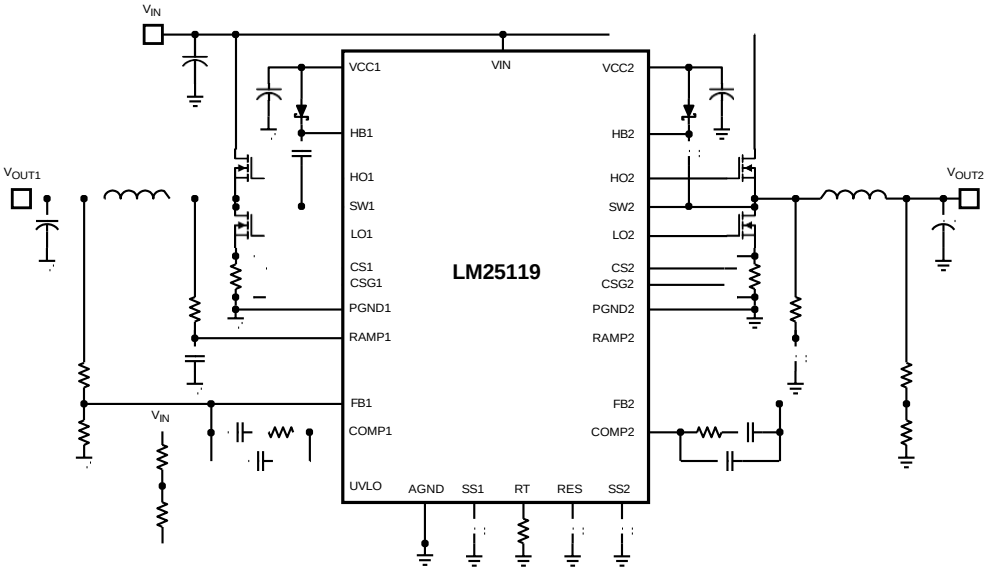
FEATURES

- **LM25119Q is an Automotive Grade product that is AEC-Q100 grade 1 qualified (-40°C to 125°C operating junction temperature).**
- **Emulated peak current mode control**
- **Wide operating range from 4.5 V to 42 V**
- **Easily configurable for dual outputs or interleaved single output**
- **Robust 3.3 A peak gate drive**
- **Switching frequency programmable to 750 kHz**
- **Optional diode emulation mode**
- **Programmable output from 0.8 V**
- **Precision 1.5% voltage reference**
- **Programmable current limit**
- **Hiccup mode overload protection**
- **Programmable soft-start**
- **Programmable line under-voltage lockout**
- **Automatic switch-over to external bias supply**
- **Channel2 enable logic input**
- **Thermal Shutdown**
- **Leadless WQFN-32 (5 mm x 5 mm) package**

DESCRIPTION

The LM25119 is a dual synchronous buck controller intended for step-down regulator applications from a high voltage or widely varying input supply. The control method is based upon current mode control utilizing an emulated current ramp. Current mode control provides inherent line feed-forward, cycle-by- cycle current limiting and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable control of very small duty cycles necessary in high input voltage applications. The switching frequency is programmable from 50 kHz to 750 kHz. The LM25119 drives external high-side and low-side NMOS power switches with adaptive dead- time control. A user-selectable diode emulation mode enables discontinuous mode operation for improved efficiency at light load conditions. A high voltage bias regulator with automatic switch-over to external bias further improves efficiency. Additional features include thermal shutdown, frequency synchronization, cycle-by-cycle and hiccup mode current limit and adjustable line under-voltage lockout. The device is available in a power enhanced leadless WQFN-32 package featuring an exposed die attach pad to aid thermal dissipation.

Typical Application Circuit



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Connection Diagram

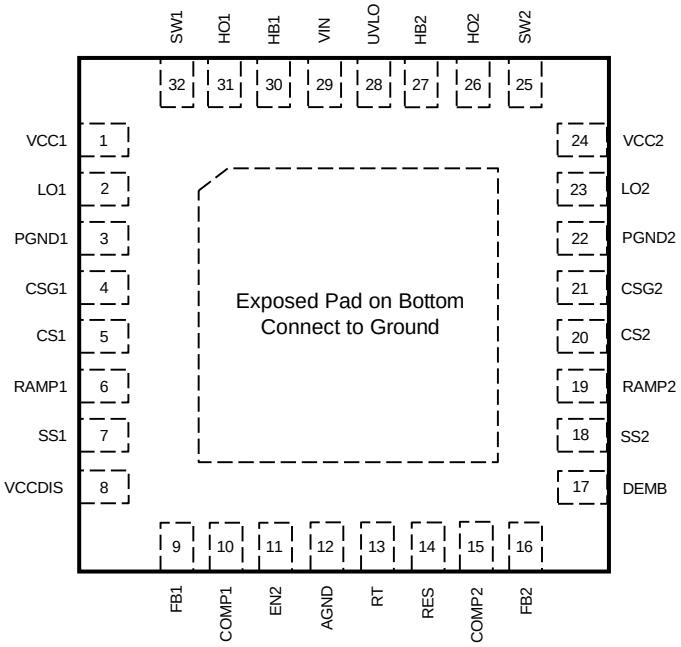

Figure 1. Top View
WQFN-32

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Pin Functions

Pin Descriptions

Pin	Name	Description
1	VCC1	Bias supply pin. Locally decouple to PGND1 using a low ESR/ESL capacitor located as close to controller as possible.
2	LO1	Low side MOSFET gate drive output. Connect to the gate of the channel1 low-side synchronous MOSFET through a short, low inductance path.
3	PGND1	Power ground return pin for low side MOSFET gate driver. Connect directly to the low side of the channel1 current sense resistor.
4	CSG1	Kelvin ground connection to the external current sense resistor. Connect directly to the low side of the channel1 current sense resistor.
5	CS1	Current sense amplifier input. Connect to the high side of the channel1 current sense resistor.
6	RAMP1	PWM ramp signal. An external resistor and capacitor connected between the SW1 pin, the RAMP1 pin and the AGND pin sets the channel1 PWM ramp slope. Proper selection of component values produces a RAMP1 signal that emulates the current in the buck inductor.
7	SS1	An external capacitor and an internal 10 µA current source set the ramp rate of the channel1 error amp reference. The SS1 pin is held low when VCC1 or VCC2 < 4 V, UVLO < 1.25 V or during thermal shutdown.
8	VCCDIS	Optional input that disables the internal VCC regulators when external biasing is supplied. If VCCDIS >1.25 V, the internal VCC regulators are disabled. The externally supplied bias should be coupled to the VCC pins through a diode. VCCDIS has a 500 kΩ pull-down resistor to ground to enable the VCC regulators when the pin is left floating. The pull-down resistor can be overridden by pulling VCCDIS above 1.25 V with a resistor divider connected to the external bias supply.
9	FB1	Feedback input and inverting input of the channel1 internal error amplifier. A resistor divider from the channel1 output to this pin sets the output voltage level. The regulation threshold at the FB1 pin is 0.8 V.
10	COMP1	Output of the channel1 internal error amplifier. The loop compensation network should be connected between this pin and the FB1 pin.
11	EN2	If the EN2 pin is low, channel2 will be disabled. Channel1 and all other functions remain active. The EN2 has a 50 kΩ pull-up resistor to enable channel2 when the pin is left floating.
12	AGND	Analog ground. Return for the internal 0.8 V voltage reference and analog circuits.
13	RT	The internal oscillator is set with a single resistor between RT and AGND. The recommended maximum oscillator frequency is 1.5 MHz which corresponds to a maximum switching frequency of 750 kHz for either channel. The internal oscillator can be synchronized to an external clock by coupling a positive pulse into RT through a small coupling capacitor.
14	RES	The restart timer pin for an external capacitor that configures the hiccup mode current limiting. A capacitor on the RES pin determines the time the controller will remain off before automatically restarting in hiccup mode. The two regulator channels operate independently. One channel may operate in normal mode while the other is in hiccup mode overload protection. The hiccup mode commences when either channel experiences 256 consecutive PWM cycles with cycle-by-cycle current limiting. After this occurs, a 10 µA current source charges the RES pin capacitor to the 1.25 V threshold which restarts the overloaded channel.
15	COMP2	Output of the channel2 internal error amplifier. The loop compensation network should be connected between this pin and the FB2 pin.
16	FB2	Feedback input and inverting input of the channel2 internal error amplifier. A resistor divider from the channel2 output to this pin sets the output voltage level. The regulation threshold at the FB2 pin is 0.8 V.
17	DEMB	Logic input that enables diode emulation when in the low state. In diode emulation mode, the low side MOSFET is latched off for the remainder of the PWM cycle when the buck inductor current reverses direction (current flow from output to ground). When DEMB is high, diode emulation is disabled allowing current to flow in either direction through the low side MOSFET. A 50 kΩ pull-down resistor internal to the LM25119 holds DEMB pin low and enables diode emulation if the pin is left floating.
18	SS2	An external capacitor and an internal 10 µA current source set the ramp rate of the channel2 error amp reference. The SS2 pin is held low when VCC1 or VCC2 < 4 V, UVLO < 1.25 V or during thermal shutdown.
19	RAMP2	PWM ramp signal. An external resistor and capacitor connected between the SW2 pin, the RAMP2 pin and the AGND pin sets the channel2 PWM ramp slope. Proper selection of component values produces a RAMP2 signal that emulates the current in the buck inductor.
20	CS2	Current sense amplifier input. Connect to the high side of the channel2 current sense resistor.
21	CSG2	Kelvin ground connection to the external current sense resistor. Connect directly to the low side of the channel2 current sense resistor.

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Pin Descriptions (continued)

Pin	Name	Description
22	PGND2	Power ground return pin for low side MOSFET gate driver. Connect directly to the low side of the channel2 current sense resistor.
23	LO2	Low side MOSFET gate drive output. Connect to the gate of the channel2 low-side synchronous MOSFET through a short, low inductance path.
24	VCC2	Bias supply pin. Locally decouple to PGND2 using a low ESR/ESL capacitor located as close to controller as possible.
25	SW2	Switching node of the buck regulator. Connect to channel2 bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET.
26	HO2	High side MOSFET gate drive output. Connect to the gate of the channel2 high-side MOSFET through a short, low inductance path.
27	HB2	High-side driver supply for bootstrap gate drive. Connect to the cathode of the channel2 external bootstrap diode and to the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high side MOSFET gate and should be placed as close to the controller as possible.
28	UVLO	Under-voltage lockout programming pin. If the UVLO pin is below 0.4 V, the regulator will be in the shutdown mode with all function disabled. If the UVLO pin is greater than 0.4 V and below 1.25 V, the regulator will be in standby mode with the VCC regulators operational, the SS pins grounded and no switching at the HO and LO outputs. If the UVLO pin voltage is above 1.25 V, the SS pins are allowed to ramp and pulse width modulated gate drive signals are delivered at the LO and HO pins. A 2 0 µA current source is enabled when UVLO exceeds 1.25 V and flows through the external UVLO resistors to provide hysteresis.
29	VIN	Supply voltage input source for the VCC regulators.
30	HB1	High-side driver supply for bootstrap gate drive. Connect to the cathode of the channel1 external bootstrap diode and to the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high side MOSFET gate and should be placed as close to controller as possible.
31	HO1	High side MOSFET gate drive output. Connect to the gate of the channel1 high-side MOSFET through a short, low inductance path.
32	SW1	Switching node of the buck regulator. Connect to channel1 bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET.
EP	EP	Exposed pad of WQFN package. No internal electrical connections. Solder to the ground plane to reduce thermal resistance.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

VIN to AGND	–0.3 to 45 V
SW1, SW2 to AGND	–3.0 to 45 V
HB1 to SW1, HB2 to SW2	–0.3 to 15 V
VCC1, VCC2 to AGND (2)	–0.3 to 15 V
FB1, FB2, DEMB, RES, VCCDIS, UVLO to AGND	–0.3 to 15 V
HO1 to SW1, HO2 to SW2	–0.3 to HB+0.3 V
LO1, LO2 to AGND	–0.3 to VCC+0.3 V
SS1, SS2 to AGND	–0.3 to 7 V
EN2, RT to AGND	–0.3 to 7 V
CS1, CS2, CSG1, CSG2 to AGND	–0.3 V to 0.3 V
PGND to AGND	–0.3 V to 0.3 V
ESD Rating HBM (3)	2 kV
Storage Temperature	–55°C to +150°C
Junction Temperature	+150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. For specifications and test conditions see the Electrical Characteristics Table.
(2) These pins must not exceed VIN.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

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Operating Ratings (1)

VIN	4.5 V to 42 V
VCC	4.5 V to 14 V
HB to SW	4.5 V to 14 V
Junction Temperature	–40°C to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. For specifications and test conditions see the Electrical Characteristics Table.

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Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature range of –40°C to +125°C. Unless otherwise specified, the following conditions apply: VIN = 12 V, VCC = 8 V, VCCDIS = 0 V, EN2 = 5 V, R_T = 25 kΩ, no load on LO and HO. Electrical characteristics are per channel where applicable. See (1), (2), and (3).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN Supply						
I_{BIAS}	VIN Operating Current	SS1 = SS2 = 0 V		6	**7.3**	mA
		VCCDIS = 2 V, SS1 = SS2 = 0 V		340	**500**	µA
I_{VCC}	VCC1 Operating Current	VCCDIS = 2 V, SS1 = SS2 = 0 V		3.9	**4.5**	mA
	VCC2 Operating Current	VCCDIS = 2 V, SS1 = SS2 = 0 V		1.4	**2.0**	mA
$I_{SHUTDOWN}$	VIN Shutdown Current	UVLO = 0 V, SS1 = SS2 = 0 V		15	**33**	µA
VCC Regulator(4)						
$V_{CC(REG)}$	VCC Regulation		**6.77**	7.6	**8.34**	V
	VCC Regulation	VIN = 4.5 V, No external load	**4.4**	4.46		V
	VCC Sourcing Current Limit	VCC = 0 V	**25**	40		mA
	VCCDIS Switch Threshold	VCCDIS Rising	**1.19**	1.25	**1.29**	V
	VCCDIS Switch Hysteresis			0.07		V
	VCCDIS Input Current	VCCDIS = 0 V		–20		nA
	VCC Under-voltage Threshold	Positive going VCC	**3.8**	4.0	**4.2**	V
	VCC Under-voltage Hysteresis			0.2		V
EN2 Input						
V_{IL}	EN2 Input Low Threshold			2.0	**1.5**	V
V_{IH}	EN2 Input High Threshold		**2.9**	2.5		V
	EN2 Input pull-up resistor			50		kΩ
UVLO						
	UVLO Threshold	UVLO Rising	**1.20**	1.25	**1.29**	V
	UVLO Hysterisis Current	UVLO = 1.4 V	**15**	20	**25**	µA
	UVLO Shutdown Threshold			0.4		V
	UVLO Shutdown Hysterisis Voltage			0.1		V
Soft Start						
	SS Current Source	SS = 0 V	**7**	10	**13**	µA
	SS Pull Down R_{DSON}			10		Ω
Error Amplifier						
V_{REF}	FB Reference Voltage	Measured at FB pin, FB = COMP	**0.788**	0.8	**0.812**	V
	FB Input Bias Current	FB = 0.8 V		1		nA
	FB Disable Threshold	Interleaved Threshold		2.5		V
	COMP VOH	Isource = 3mA	**2.8**			V
	COMP VOL	Isink = 3mA			**0.31**	V
A_{OL}	DC Gain			80		dB
f_{BW}	Unity Gain Bandwidth			3		MHz
PWM Comparators						
$t_{HO(OFF)}$	Forced HO Off-time		**220**	320	**430**	ns
$t_{ON(min)}$	Minimum HO On-time	C_{RAMP} = 50 pF		100		ns

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. For specifications and test conditions see the Electrical Characteristics Table.
(2) All limits are specified. All electrical characteristics having room temperature limits are tested during production at T_A = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Texas Instrument's Average Outgoing Quality Level (AOQL).
(4) Per VCC Regulator

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Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature range of –40°C to +125°C. Unless otherwise specified, the following conditions apply: VIN = 12 V, VCC = 8 V, VCCDIS = 0 V, EN2 = 5 V, R_T = 25 kΩ, no load on LO and HO. Electrical characteristics are per channel where applicable. See (1), (2), and (3).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Oscillator						
f_{SW1}	Frequency 1	R_T = 25 kΩ	**180**	200	**220**	kHz
f_{SW2}	Frequency 2	R_T = 10 kΩ	**430**	480	**530**	kHz
	RT Output Voltage			1.25		V
	RT Sync Positive Threshold		**2.5**	3.2	**4**	V
	Sync Pulse Minimum Width		**100**			ns
Current Limit						
$V_{CS(TH)}$	Cycle-by-cycle Sense Voltage Threshold (CS - CSG)	RAMP = 0	**106**	120	**134**	mV
	CS Bias Current	CS = 0 V		-70	**–95**	µA
	Hiccup Mode Fault Timer			256		Cycles
RES						
I_{RES}	RES current Source			9.7		µA
V_{RES}	RES threshold	C_{RES} Charging	**1.20**	1.25	**1.30**	V
Diode Emulation						
V_{IL}	DEMB Input Low Threshold			2.0	**1.65**	V
V_{IH}	DEMB Input High Threshold		**2.9**	2.6		V
	DEMB Input Pull-Down Resistance			50		kΩ
	SW Zero Cross Threshold			–5		mV
LO Gate Driver						
V_{OLL}	LO Low-state Output Voltage	I_{LO} = 100mA		0.1	**0.18**	V
V_{OHL}	LO High-state Output Voltage	I_{LO} = –100mA, V_{OHL} = VCC - V_{LO}		0.17	**0.26**	V
	LO Rise Time	C-load = 1000 pF		6		ns
	LO Fall Time	C-load = 1000 pF		5		ns
I_{OHL}	Peak LO Source Current	V_{LO} = 0 V		2.5		A
I_{OLL}	Peak LO Sink Current	V_{LO} = VCC		3.3		A
HO Gate Driver						
V_{OLH}	HO Low-state Output Voltage	I_{HO} = 100 mA		0.11	**0.19**	V
V_{OHH}	HO High-state Output Voltage	I_{HO} = –100 mA, V_{OHH} = V_{HB} V_{HO}		0.18	**0.27**	V
	HO Rise Time	C-load = 1000 pF		6		ns
	HO Fall Time	C-load = 1000 pF		5		ns
I_{OHH}	Peak HO Source Current	V_{HO} = 0 V, SW = 0, HB = 8 V		2.2		A
I_{OLH}	Peak HO Sink Current	V_{HO} = V_{HB} = 8 V		3.3		A
	HB to SW Under-voltage			3		V
	HB DC Bias Current	HB - SW = 8 V		70	**100**	µA
SWITCHING CHARACTERISTICS						
	LO Fall to HO Rise Delay	No load		70		ns
	HO Fall to LO Rise Delay	No load		60		ns
THERMAL						
T_{SD}	Thermal Shutdown	Rising		165		°C
	Thermal Shutdown Hysteresis			25		°C
θ_{JA}	Junction to Ambient			40		°C/W
θ_{JC}	Junction to Case			4		°C/W

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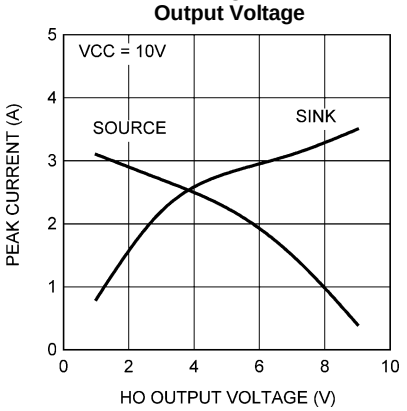
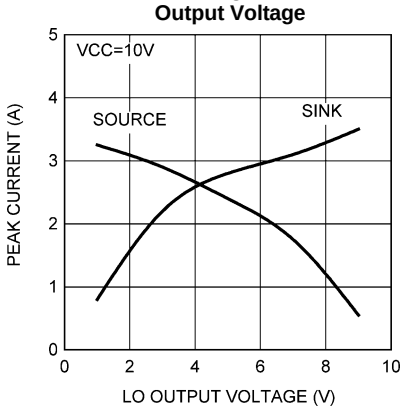
Typical Performance Characteristics

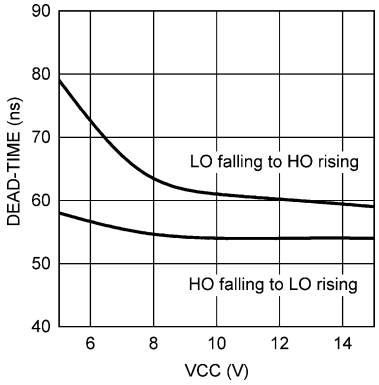
HO Peak Driver Current vs Output Voltage



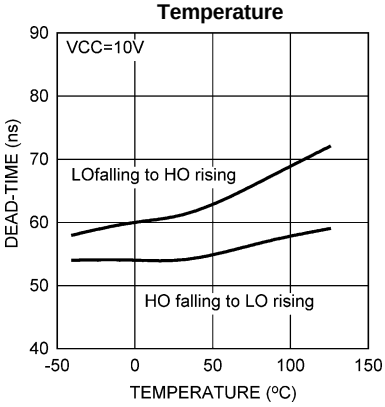
LO Peak Driver Current vs Output Voltage



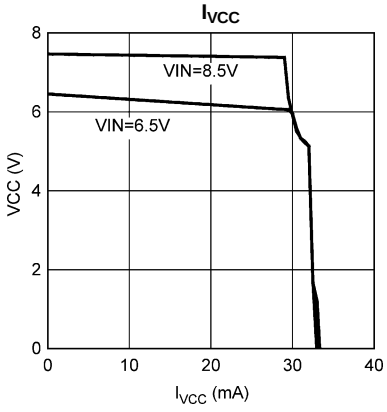
Driver Dead Time vs VCC



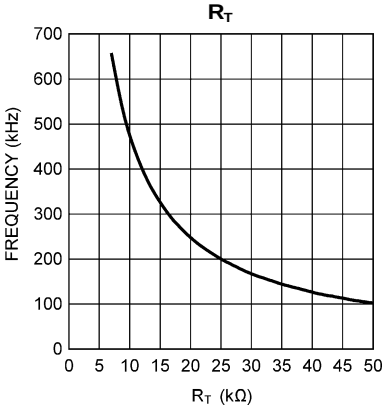
Driver Dead Time vs Temperature



VCC vs I_{VCC}



Switching Frequency vs R_T



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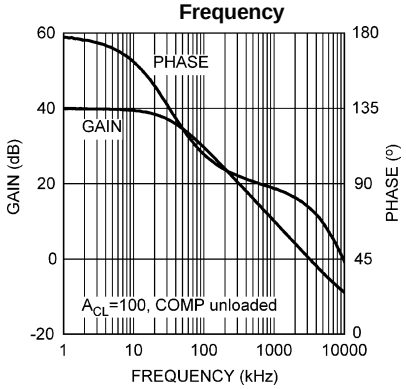
Typical Performance Characteristics (continued)

Error Amp Gain and Phase vs Frequency



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Block Diagram

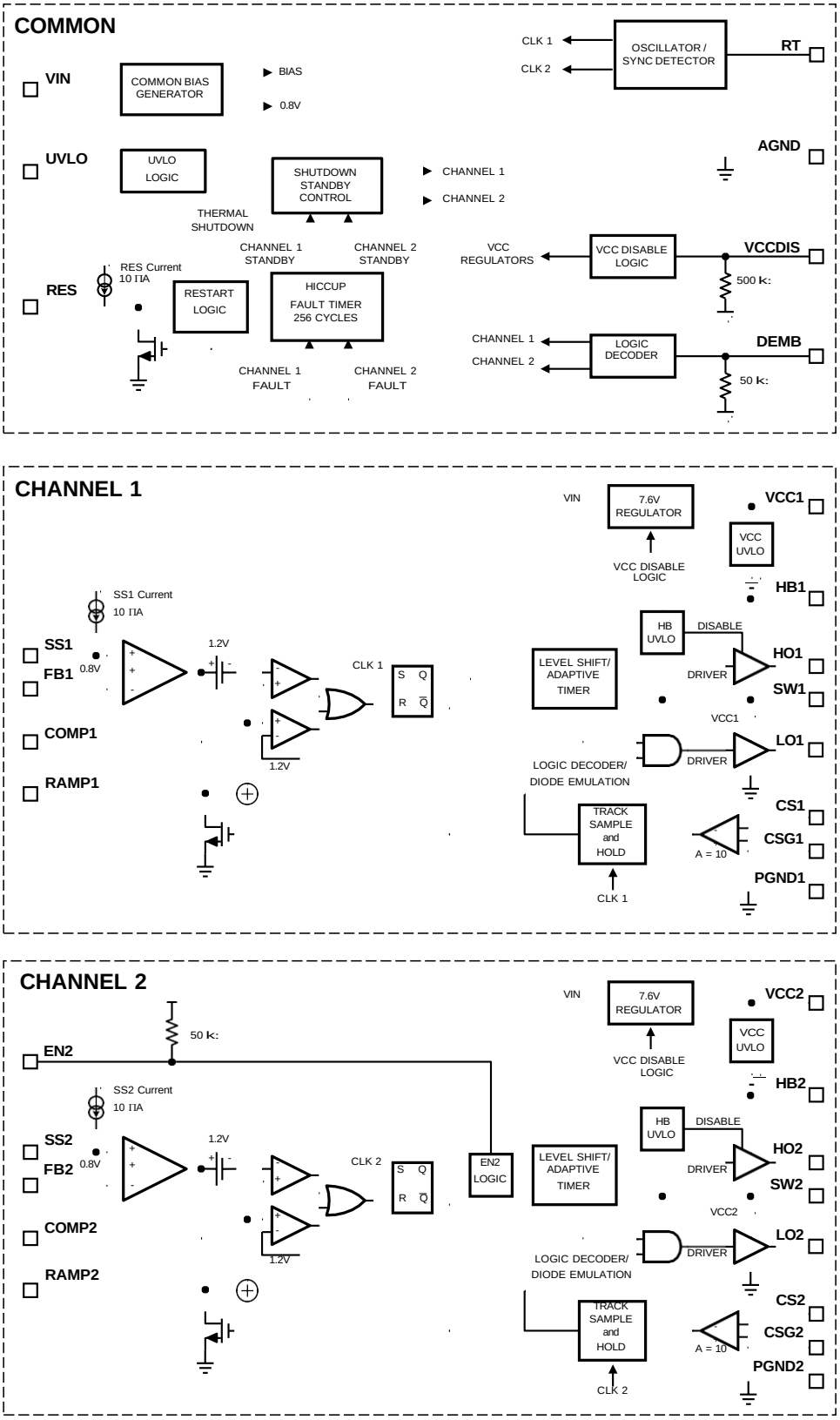

Figure 2. Block Diagram

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