Multi-Phase PWM Controller

The ISL6244 provides core-voltage regulation by driving 2 to 4 interleaved synchronous-rectified buck-converter channels in parallel. Interleaving the channel timing results in increased ripple frequency which reduces input and output ripple currents. The reduction in ripple results in lower component cost, reduced dissipation, and a smaller implementation area.

The ISL6244 uses cost and space-saving $r_{DS(ON)}$ sensing for channel current balance, active voltage positioning, and over-current protection. Output voltage is monitored by an internal differential remote sense amplifier. A high-bandwidth error amplifier drives the output voltage to match the programmed 5-bit DAC reference voltage. The resulting compensation signal guides the creation of pulse width modulated (PWM) signals to control companion Intersil MOSFET drivers. The OFS pin allows direct offset of the DAC voltage from 0V to 100mV using a single external resistor. The entire system is trimmed to ensure a system accuracy of ±1%.

Outstanding features of this controller IC include Dynamic VID™ technology allowing seamless on-the-fly VID changing without the need of any external components. Battery “feed-forward” is provided to allow for traditional control schemes over total input voltage variation. Output voltage “droop” or active voltage positioning is optional. When employed, it allows the reduction in size and cost of the output capacitors required to support load transients. A threshold-sensitive enable input allows the use of an external resistor divider for start-up coordination with Intersil MOSFET drivers or any other devices powered from a separate supply.

Superior over-voltage protection is achieved by gating on the lower MOSFET of all phases to reduce the output voltage. Under-voltage conditions are detected, but PWM operation is not disrupted. Over-current conditions cause a hiccup-mode response as the controller repeatedly tries to restart. After a set number of failed startup attempts, the controller latches off. A power good logic signal indicates when the converter output is between the UV and OV thresholds.

Features

- Multi-Phase Power Conversion
  - 2, 3 or 4 Phase Operation
- Active Channel Current Balancing
- Precision $r_{DS(ON)}$ Current Sharing
  - Lossless
  - Low Cost
- Precision CORE Voltage Regulation
  - Differential Remote Output Voltage Sensing
  - Programmable Reference Offset
  - ±1% System Accuracy
- Microprocessor Voltage Identification Input
  - 5-Bit VID Input
  - 0.800V to 1.550V in 25mV Steps
  - Dynamic VID Technology
- Programmable Droop Voltage
- Excellent Dynamic Response
  - Combined Input Voltage Feed-Forward and Pulse-by-Pulse Average Current Mode
- Over Current Protection
- Digital Soft Start
- Threshold Sensitive Enable Input
- High Ripple Frequency (160kHz to 4MHz)
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free Available (RoHS Compliant)

Applications

- AMD Hammer Family Processor Voltage Regulator
- Low Output Voltage, High Current DC-DC Converters
- Voltage Regulator Modules

Ordering Information

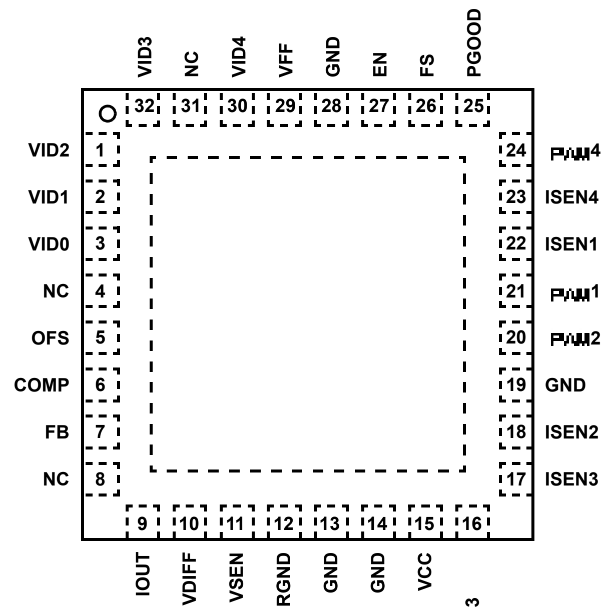
PART NUMBER	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL6244CR	0 to 70	32 Ld 5x5 QFN	L32.5x5
ISL6244CRZ (Note 1)	0 to 70	32 Ld 5x5 QFN (Pb-free)	L32.5x5
ISL6244HR	-10 to 100	32 Ld 5x5 QFN	L32.5x5
ISL6244HRZ (Note 1)	-10 to 100	32 Ld 5x5 QFN (Pb-free)	L32.5x5

NOTES:

1. Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add “-T” suffix for 32 QFN 5x5 Tape and Reel packages.

Pinout

ISL6244CR
(32 LEAD QFN 5x5)
TOP VIEW



NC = NO CONNECT

Absolute Maximum Ratings

Supply Voltage, VCC (Note 3) . . . .+7V
Input, Output, or I/O Voltage . . . . GND -0.3V to V_{CC} + 0.3V
ESD Classification . . . . .Class II

Operating Conditions

Supply Voltage, VCC . . . . +5V ±5%
Ambient Temperature. . . . .-10°C to 100°C
Maximum Junction Temperature . . . . .125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 4, 6).	32	4

Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range. . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

3. For VCC > 5.5V, current must be limited to 25mA.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. Tolerance does not include the VID offset error or any external component tolerances.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VCC = 5V, T_A = -10°C to 100°C. Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT					
Nominal Supply	VCC = 5VDC; EN = 5VDC; R_T = 100kΩ ±1%	8.0	10.8	14.0	mA
Shutdown Supply	VCC = 5VDC; EN = 0VDC; R_T = 100kΩ ±1%	8.0	10.3	13.0	mA
POWER-ON RESET AND ENABLE					
POR Threshold	VCC Rising	4.25	4.35	4.60	V
	VCC Falling	3.75	3.85	4.00	V
ENABLE Threshold	EN Rising	1.215	1.240	1.265	V
	Hysteresis	82	92	102	mV
REFERENCE VOLTAGE AND DAC					
System Accuracy (Note 5)		-1.2	-	1.2	%VID
	0 to 70°C	-1	-	1	%VID
VID on Fly Step Size	R_T = 100kΩ	-	25	-	mV
VID Pull Up		-30	-20	-10	μA
VID Input Low Level		-	-	0.8	V
VID Input High Level		2.0	-	-	V
PIN-ADJUSTABLE OFFSET					
OFS Current		-	100	-	μA
Offset Accuracy	ROFS = 5kΩ ±1%	92.0	100.0	108.0	mV
	ROFS = 5kΩ ±1% , 0 to 70°C	94.0	100.0	106.0	
Maximum Offset		-	-	100.0	mV
OSCILLATOR					
Accuracy		-12.5	-	12.5	%
	RT = 100K	245	280	315	kHz
Adjustment Range		0.08	-	1.0	MHz
VFF Range		0.5	-	2.5	V
Max Duty Cycle		-	75	-	%

Electrical Specifications Operating Conditions: VCC = 5V, T_A = -10°C to 100°C. Unless Otherwise Specified. (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER					
Open-Loop Gain	R_L = 10kΩ to ground	-	72	-	dB
Open-Loop Bandwidth	C_L = 100pF, R_L = 10kΩ to ground	-	18	-	MHz
Slew Rate	C_L = 100pF, Load = ±400mA	3	7.1	11	V/µs
Maximum Output Voltage	R_L = 10kΩ to ground	3.6	4.5	-	V
Source Current		3.0	7.0	11.5	mA
Sink Current		1.6	3.0	5.4	mA
REMOTE-SENSE AMPLIFIER					
Input Impedance		-	80	-	kΩ
Bandwidth		-	20	-	MHz
Slew Rate		-	6	-	V/µs
SENSE CURRENT					
IOUT Accuracy	ISEN1 = ISEN2 = ISEN3 = ISEN4 = 50µA	-5	-	5	%
ISEN Offset Voltage		-	6	-	mV
Over-Current Trip Level		68	85	102	µA
POWER GOOD AND PROTECTION MONITORS					
PGOOD Low Voltage	I_{PGOOD} = 4mA	-	-	0.4	V
Under-Voltage Offset From VID	VSEN Falling	320	370	420	mV
Over-Voltage Threshold	VSEN Rising	2.08	2.13	2.20	V

Typical Operating Performance

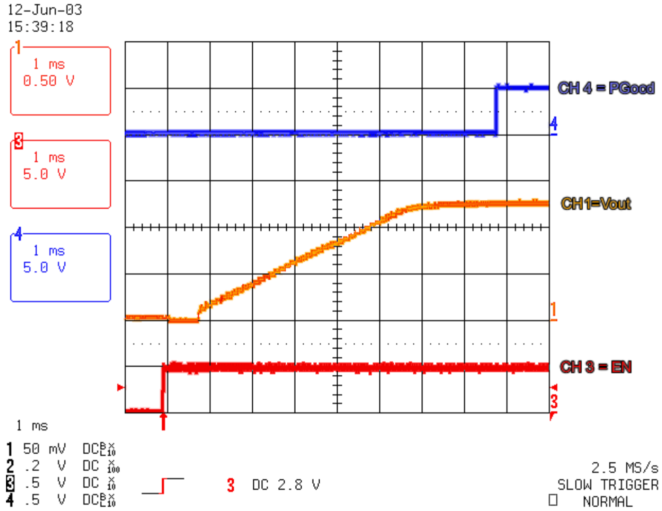


FIGURE 1. SOFT-START WAVEFORM

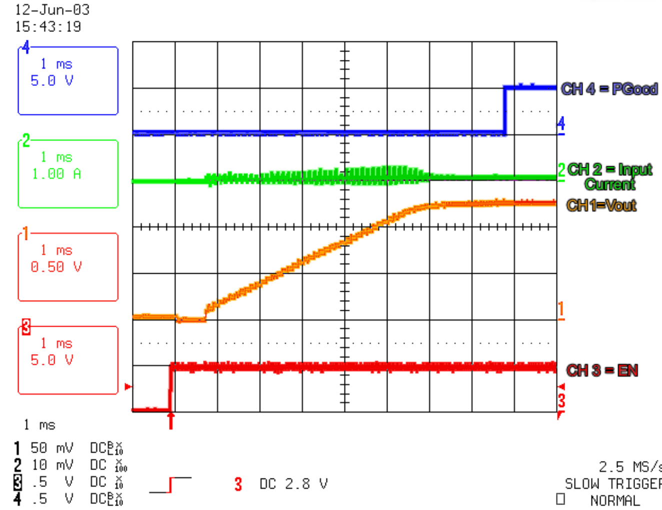


FIGURE 2. INRUSH CURRENT AT VIN 19V @ 52A

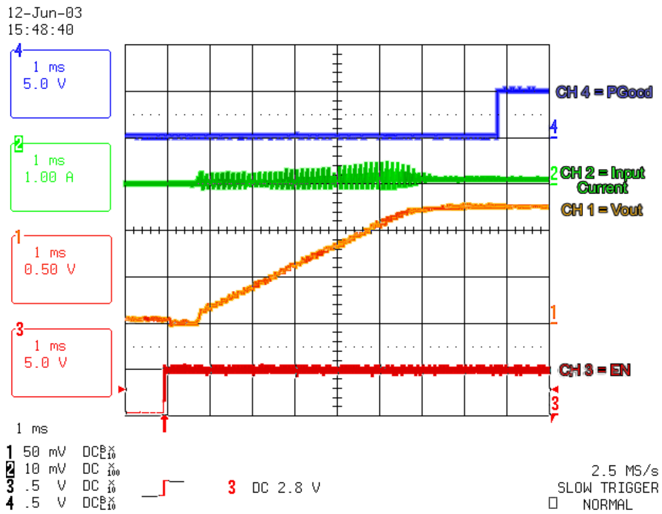


FIGURE 3. INRUSH CURRENT AT VIN 10.8V @ 52A

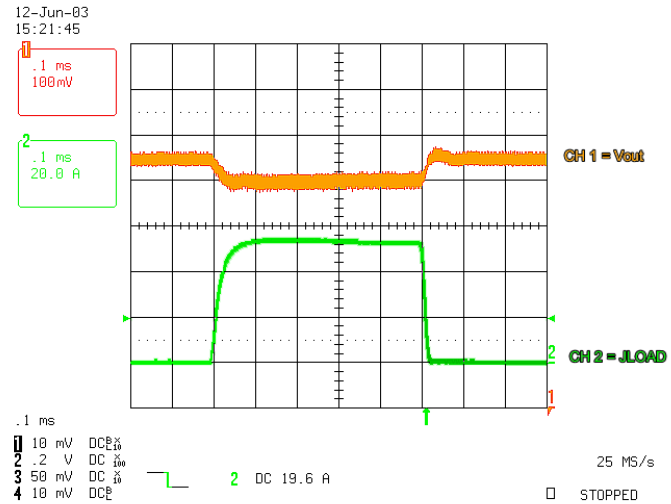


FIGURE 4. TRANSIENT WAVEFORM FROM 0A TO 52A

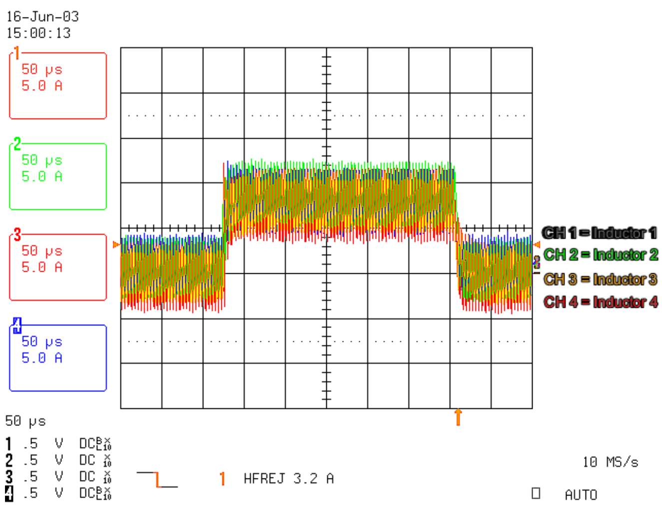


FIGURE 5. INDUCTOR CURRENT TRANSIENT

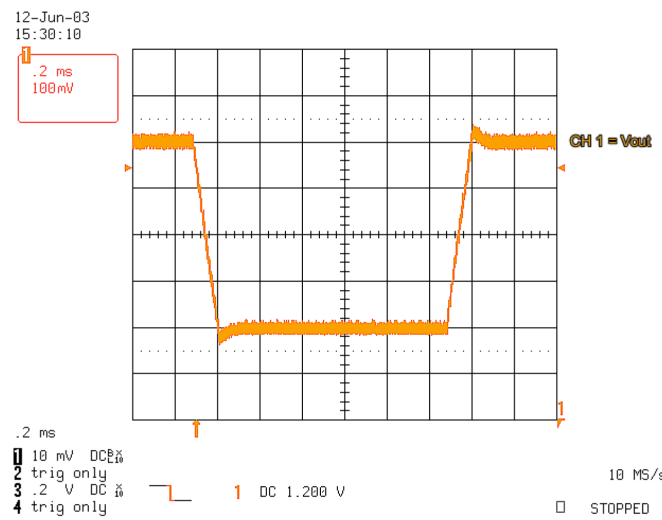


FIGURE 6. VID CHANGES FROM 1.60V TO 1.20V

Typical Operating Performance

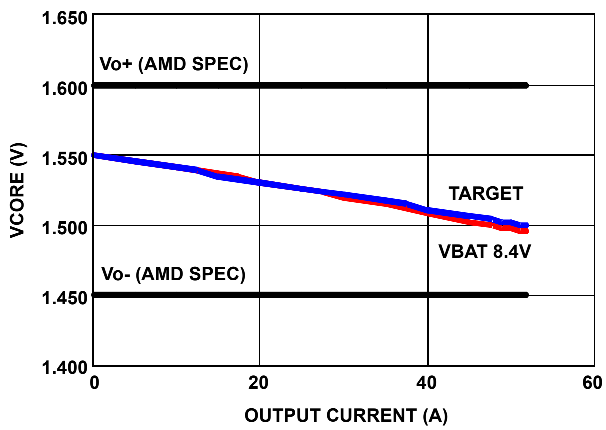


FIGURE 7. ISL6244 DROOP: V_{BAT} = 8.4V

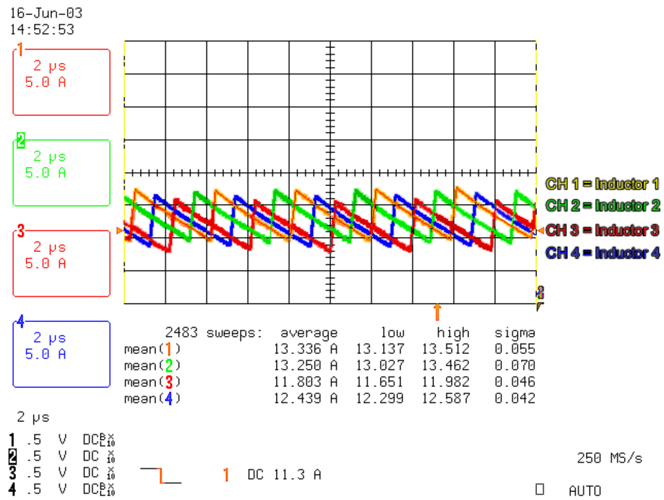


FIGURE 8. FOUR PHASE CURRENT BALANCE @ 52A

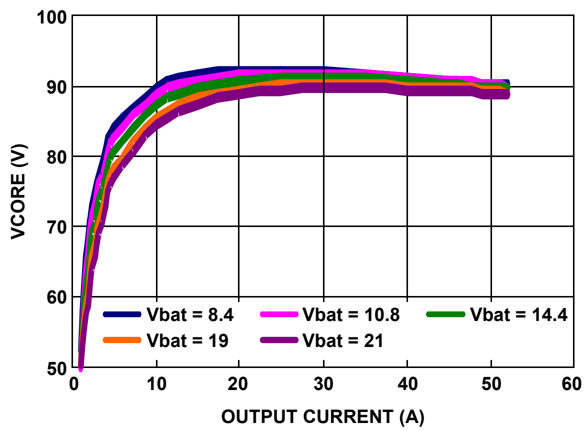


FIGURE 9. ISL6244 EFFICIENCY vs LOAD

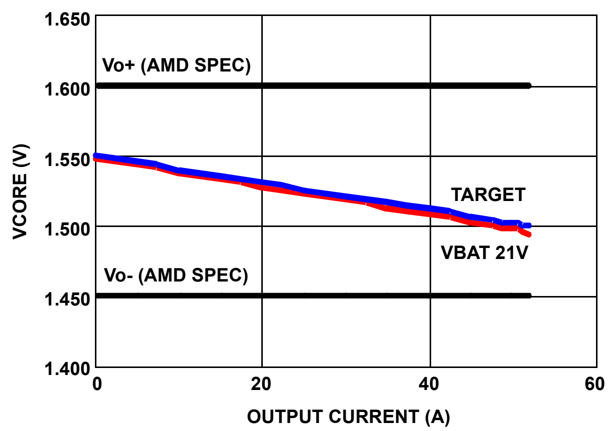
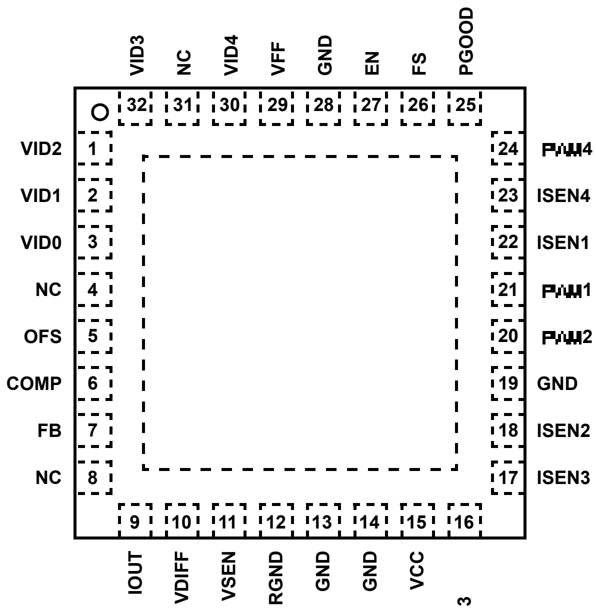


FIGURE 10. ISL6244 DROOP: V_{BAT} = 21V

Functional Pin Description

ISL6244CR
(32 LEAD QFN 5x5)
TOP VIEW



NC = NO CONNECT

GND

Bias and reference ground for the IC.

VFF

This pin is connected to VIN through a 10:1 voltage divider to allow for battery "feed-forward," which improves stability over varying input line.

VID4, VID3, VID2, VID1, VID0

The state of these five inputs program the internal DAC, which provides the reference voltage for output regulation. Connect these pins to either open-drain or active pull-up type outputs. Pulling these pins above 2.9V can cause a reference offset inaccuracy.

OFS

Connecting a resistor between this pin and ground creates a positive offset voltage which is added to the DAC voltage, allowing easy implementation of load-line regulation. For no offset, simply tie this pin to ground.

FB and COMP

The internal error amplifier inverting input and output respectively. Connect the external R-C feedback compensation network of the regulator to these pins.

IOUT

The current carried out of this pin is proportional to o[illegible] current and can be used to incorporate output voltage droop and/or load sharing. The scale factor is set by the ratio of the ISEN resistors and the lower MOSFET $r_{DS(ON)}$. If droop is desired, connect this pin to FB. When not used for droop or load sharing, simply leave this pin open.

VSEN, RGND, VDIFF

VSEN and RGND are the inputs to the differential remote-sense amplifier. Connect these pins to the sense points of the remote load. Connect an appropriately sized feedback resistor, R_{FB}, between VDIFF and FB.

VCC

Supplies all the power necessary to operate the chip. The IC starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. Connect this pin directly to a +5V supply.

ISEN1, ISEN2, ISEN3, ISEN4

Current sense inputs. A resistor connected between these pins and their respective phase node sets a current proportional to the current in the lower MOSFET during it's conduction interval. This current is used as a reference for channel balancing, load sharing, protection, and load-line regulation. Inactive channels should have their respective sense inputs left open.

PWM1, PWM2, PWM3, PWM4

Pulse-width modulating outputs. Connect these pins to the individual ISL620X driver PWM input pins. These logic outputs command the driver IC(s) in switching the half-bridge configuration of MOSFETs. The number of active channels is determined by the state of PWM3 and PWM4. If PWM3 is tied to VCC, this indicates to the controller that two channel operation is desired. In this case, PWM 4 should be left open or tied to VCC. Shorting PWM4 to VCC indicates that three channel operation is desired.

PGOOD

Power good is an open-drain logic output that changes to a logic low when the voltage at VDIFF is 350mV below the VID setting (under-voltage) or above 2.2V (over-voltage).

FS

A pin for setting the switching frequency of the regulator. Place a resistor from this pin to ground to set the switching frequency between 80kHz and 1MHz.

EN

This pin enables the ISL6244 regulator.

Typical Application: 3-Phase Buck Converter with $r_{DS(ON)}$ Current Sensing

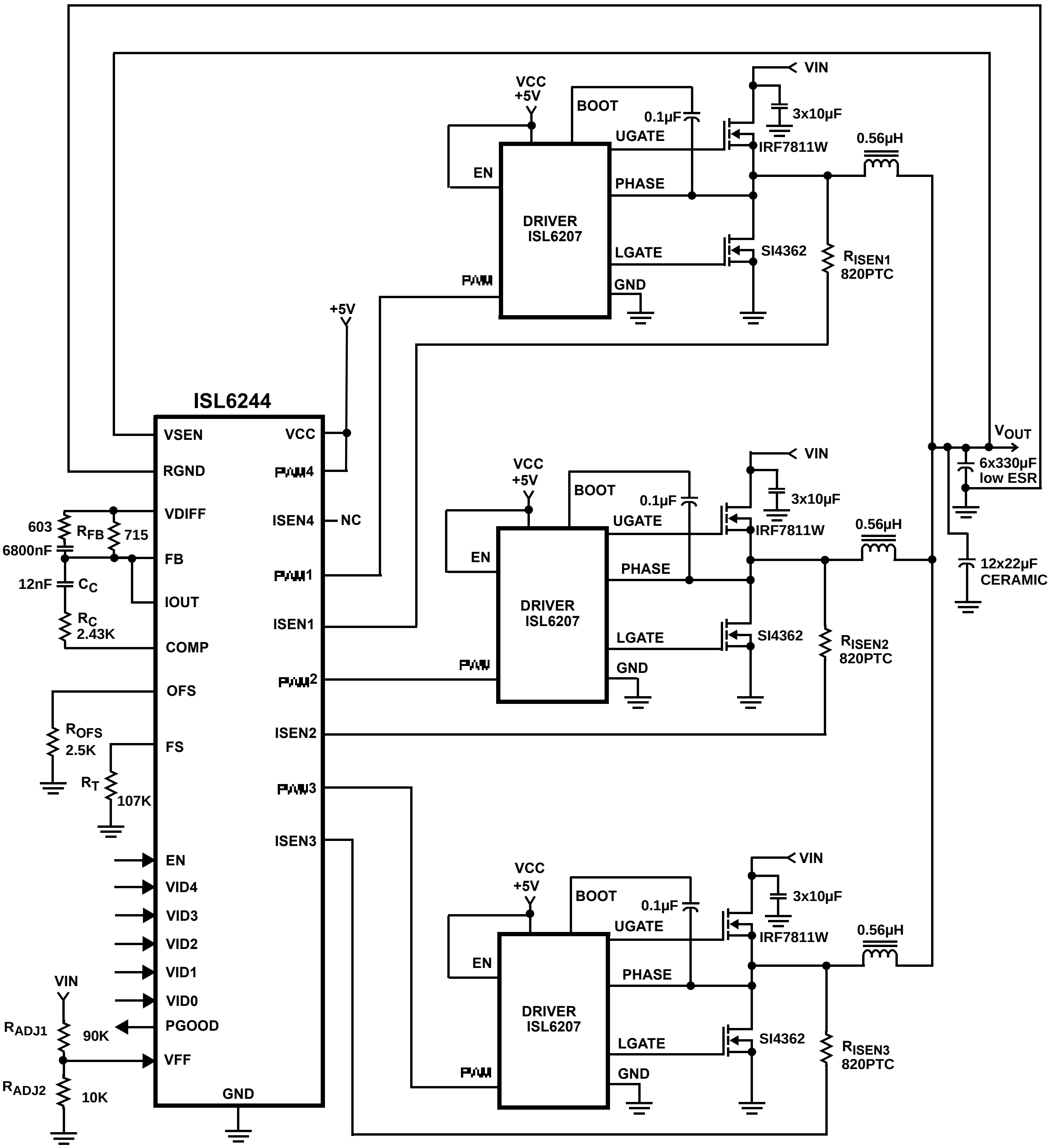


FIGURE 11. TYPICAL APPLICATION

Theory of Operation

Multi-Phase Power Conversion

Microprocessor load current profiles have changed to the point where the multi-phase power conversion advantage is pronounced. The technical challenges associated with producing a single-phase converter which is both cost-effective and thermally viable have forced a change t[illegible] cost-saving approach of multi-phase. The ISL6244 c[illegible] helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The block diagram in Figure 12 provides a top level view of multi-phase power conversion using the ISL6244 controller.

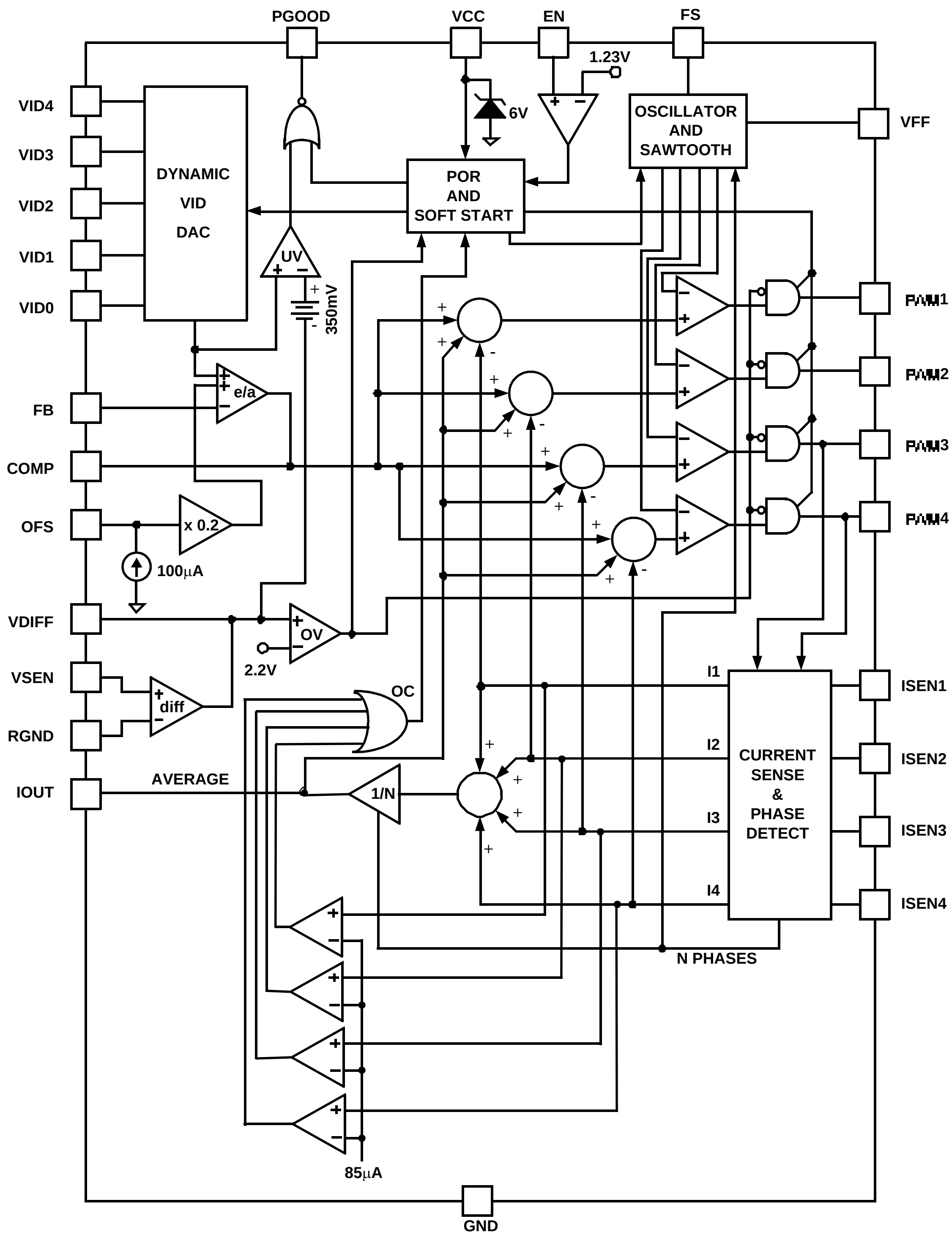


FIGURE 12. BLOCK DIAGRAM

Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

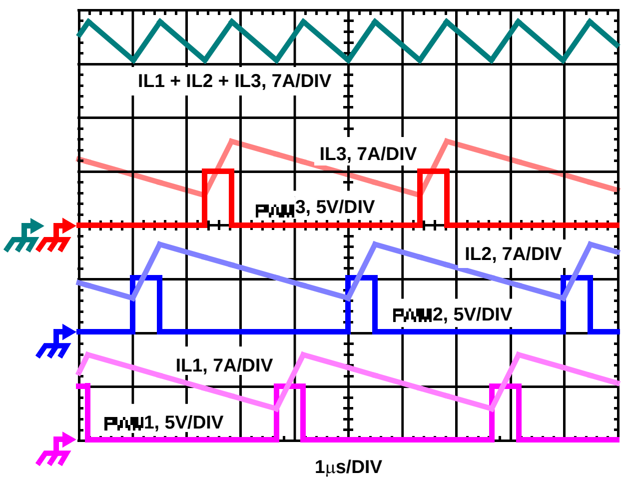


FIGURE 13. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

Figure 13 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3), combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle, or 1.33µs for f_S = 250kHz, after the PWM pulse of the previous phase. The peak-to-peak current waveforms for each phase is about 7A, and the dc components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multi-phase circuit, examine the equation representing an individual channel's peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{L f_S V_{IN}} \qquad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,PP} = \frac{(V_{IN} - N\,V_{OUT})V_{OUT}}{L f_S V_{IN}} \qquad \text{(EQ. 2)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 14 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

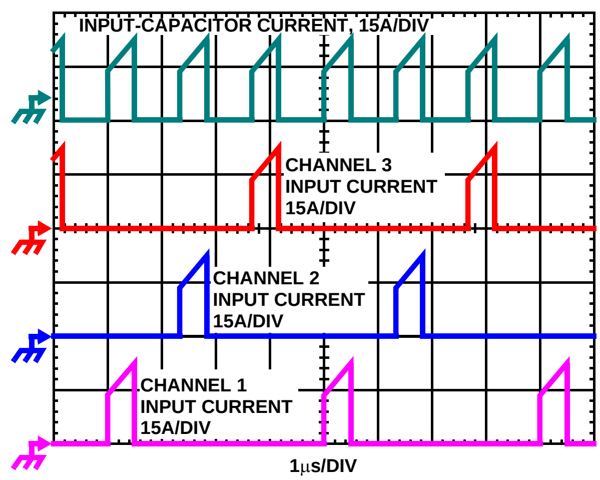


FIGURE 14. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

The converter depicted in Figure 14 delivers 52A to a 1.20V load from a 19V input. The RMS input capacitor current is 6.5A. Compare this to a single-phase converter also stepping down 19V to 1.20V at 52A. The single-phase converter has 11.96A RMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

Figures 28, 29 and 30 in the section entitled *Input Capacitor Selection* can be used to determine the input-capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution. Figure 31 shows the single phase input-capacitor RMS current for comparison.