Intel® FPGA SDK for OpenCL™

Intel® Arria® 10 SoC Development Kit Reference Platform Porting Guide

Updated for Intel® Quartus® Prime Design Suite: **19.1**

Online Version
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1. Intel® FPGA SDK for OpenCL™ Intel® Arria® 10 SoC Development Kit Reference Platform Porting Guide

The *Intel® Arria® 10 SoC Development Kit Reference Platform Porting Guide* describes the procedures and design considerations for modifying the Intel Arria 10 SoC Development Kit Reference Platform (a10soc) into your own Custom Platform for use with the Intel FPGA SDK for OpenCL™ [1] [2] SDK.

1.1. Intel Arria 10 SoC Development Kit Reference Platform: Prerequisites

The *Intel Arria 10 SoC Development Kit Reference Platform Porting Guide* assumes that you are an experienced FPGA designer who is familiar with Intel's FPGA design tools and concepts.

Prerequisites for the a10soc Reference Platform:

- An Intel Arria 10 SoC-based accelerator card with working memory interfaces

  Test these interfaces together in the same design using the same version of the Intel Quartus® Prime Pro Edition software that you will use to develop your Custom Platform.
- Intel Quartus Prime Pro Edition software Version 19.3
- Designing with Logic Lock Plus regions
- Intel SoC Embedded Design Suite Version 19.3

General knowledge prerequisites:

- FPGA architecture, including clocking, global routing, and I/Os
- High-speed design
- Timing analysis
- Platform Designer design, and Avalon® and AXI interfaces
- Tcl scripting
- Hard processor systems (HPS)
- DDR4 external memory
- Embedded Linux development

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[1] OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.

[2] The Intel FPGA SDK for OpenCL is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

This document also assumes that you are familiar with the following Intel FPGA SDK for OpenCL-specific tools and documentation:

- Custom Platform Toolkit and the *Intel FPGA SDK for OpenCL Custom Platform Toolkit User Guide*
- *Intel FPGA SDK for OpenCL Intel Arria 10 GX FPGA Development Kit Reference Platform Porting Guide*
- *Intel FPGA SDK for OpenCL Cyclone V SoC Development Kit Reference Platform Porting Guide*

Related Information

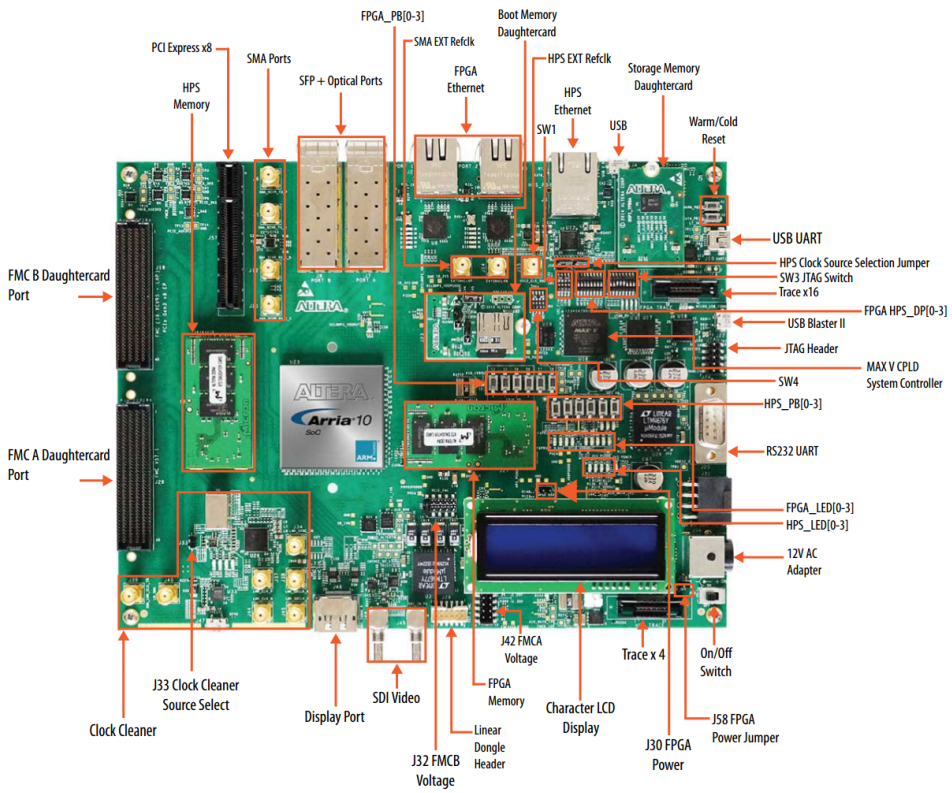
- Intel FPGA SDK for OpenCL Custom Platform Toolkit User Guide
- Intel FPGA SDK for OpenCL Intel Arria 10 GX FPGA Development Kit Reference Platform Porting Guide
- Intel FPGA SDK for OpenCL Intel Cyclone V SoC Development Kit Reference Platform Porting Guide
- Intel FPGA SDK for OpenCL Intel Stratix V Network Reference Platform Porting Guide

1.2. Features of the Intel Arria 10 SoC Development Kit Reference Platform

Prior to designing an Intel FPGA SDK for OpenCL Custom Platform, decide on design considerations that allow you to fully utilize the available hardware on your computing card.

The Intel Arria 10 SoC Development Kit Reference Platform targets a subset of the hardware features available in the Intel Arria 10 SoC Development Kit.

Figure 1. Hardware Features of the Intel Arria 10 SoC Development Kit



Features of the a10soc Reference Platform:

- OpenCL Host

  The a10soc Reference Platform uses the Intel SoC HPS as the host that connects to the FPGA fabric via HPS-to-FPGA (H2F) and FPGA-to-HPS (F2H) bridges.

- OpenCL Global Memory

  The hardware provides two 1-gigabyte (GB) DDR4 SDRAM daughtercards that are mounted on the HiLo connectors (HPS Memory and FPGA Memory in Figure 1 on page 5).

- FPGA Programming via Partial Reconfiguration (PR) over HPS lightweight bridge (Lw-bridge)

- Guaranteed Timing

The a10soc Reference Platform relies on the Intel Quartus Prime Pro Edition compiler to provide guaranteed timing closure. The timing-clean a10soc Reference Platform is preserved in the form of a precompiled post-fit netlist (that is, the `base.qdb` Intel Quartus Prime Partition Database File that is part of the `base.qar` Intel Quartus Prime Archive File). The Intel FPGA SDK for OpenCL Offline Compiler imports this preserved post-fit netlist into each OpenCL kernel compilation.