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## 摘 要

本篇论文所讲述的是对电力谐波的检测与分析问题。由于电力技术的快速发展，电力谐波的危害越来越严重，所以展开对电力谐波的检测分析就显得迫在眉睫，十分重要。一旦找到减少电力谐波危害的方法，对于工业生产和家庭用电等各方面都有着十分重要的意义和价值。

本设计的基本思路是运用快速傅里叶变换（FFT）算法进行电力谐波检测，其中关键是对电力信号进行分析的 FFT 模块用 FPGA 进行设计实现。本文的设计思路是从电网采集中得到一个高电信号，通过信号调理电路，其由霍尔传感器、低通滤波器、偏置电路组成。通过该模块将强电信号转换成弱电信号，将其信号转送到模/数转换器，通过 ADC 将连续的模拟信号转变成离散的数字信号，最后将转换后的数字信号送入 FPGA 进行 FFT 运算的数据处理。其中采用 FFT 算法难免会产生频谱泄漏、栅栏效应、频谱混叠现象，本文通过采用锁相环倍频电路来进行修正，随时调整输入模数转换器之中的频率，从而减少频谱混叠现象。

另外本文着重介绍了如何用 FPGA 进行 FFT 模块的设计，采用了按时域抽取的算法，减少了计算的复杂量，最后用 Quartus II 进行了 FFT 处理器仿真验证，完全符合电力谐波检测分析的设计需求。

**关键词：**电力谐波；FFT；锁相环；FPGA

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## Abstract

This paper is about the detection and analysis of power harmonics. Because of the rapid development of power technology, the harm of power harmonics is more and more serious, so it is urgent and very important to carry out the detection and analysis of power harmonics. Once we find a way to reduce the harm of power harmonics, it has a very important significance and value for industrial production and household electricity.

The basic idea of this design is to use fast Fourier transform (FFT) algorithm to detect power harmonics, and the key is to design and implement FFT module for power signal analysis with FPGA. The design idea of this paper is to get a high-voltage signal from the power grid collection. Through the signal conditioning circuit, it is composed of Hall sensor, low-pass filter and bias circuit. Through this module, the strong electric signal is converted into the weak electric signal, the signal is transferred to the analog-to-digital converter, the continuous analog signal is converted into discrete digital signal by ADC, and finally the converted digital signal is sent to FPGA for FFT data processing. The FFT algorithm will inevitably produce spectrum leakage, fence effect and spectrum aliasing. In this paper, the frequency of the input ADC is adjusted at any time by using the PLL frequency doubling circuit to reduce the spectrum aliasing.

In addition, this paper focuses on how to use FPGA to design FFT module, uses the algorithm of time-domain extraction, reduces the complexity of calculation, and finally uses Quartus II to carry out FFT processor simulation verification, which fully meets the design requirements of power harmonic detection and analysis.

**Keywords:** Power harmonics; FFT; phase-locked loop; FPGA

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