

F-Tile Interlaken Intel[®] FPGA IP Design Example User Guide

Updated for Quartus[®] Prime Design Suite: **24.2**

IP Version: **8.1.0**



Online Version



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1. Quick Start Guide

The F-Tile Interlaken Intel® FPGA IP provides a simulation testbench and a hardware design example that supports compilation and hardware testing. When you generate the design example, the parameter editor automatically creates the files necessary to simulate, compile, and test the design.

The testbench and design example supports NRZ and PAM4 mode for F-tile devices. The F-Tile Interlaken Intel FPGA IP generates design examples for the following supported combinations of number of lanes and data rates.

Table 1. IP Supported Physical Combinations of Number of Lanes and Data Rates

The IP supports the following combinations in the Quartus® Prime Pro Edition software version 24.2.

For FGT PAM4 transceiver mode:

- Physical configuration of 2 lanes x 53.125 Gbps, corresponds to IP GUI settings 4 lanes x 26.5625 Gbps.
- Physical configuration of 10 lanes x 56.25 Gbps, corresponding to IP GUI settings 20 lanes x 28.125 Gbps.

For FHT PAM4 transceiver mode:

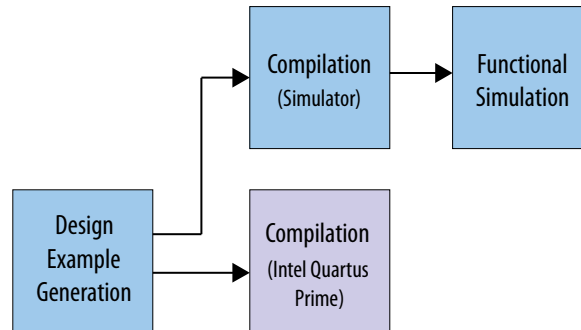
- Physical configuration of 1 lane x 106.25 Gbps, corresponds to IP GUI settings 4 lanes x 26.5625 Gbps.

Number of Lanes	Lane Rate (Gbps)						
	6.25	10.3125	12.5	25.78125	53.125	56.25	106.25
1	-	-	-	-	-	-	Yes
2	-	-	-	-	Yes	-	Yes
3	-	-	-	-	-	-	Yes
4	Yes	-	Yes	Yes	Yes	-	Yes
6	-	-	-	Yes	Yes	-	-
8	-	Yes	Yes	Yes	Yes	-	-
10 ⁽¹⁾	-	-	Yes	Yes	Yes	Yes	-
12	-	Yes	Yes	Yes	Yes	Yes	-

Note: For designs with 56.25 Gbps data rate, you may observe a minimum pulse width violation when using a device with a speed grade of -3.

⁽¹⁾ For a 10-lane configuration design, the F-Tile requires 12 lanes of TX PMA to enable bonded transceiver clocking for minimizing the channel skew.

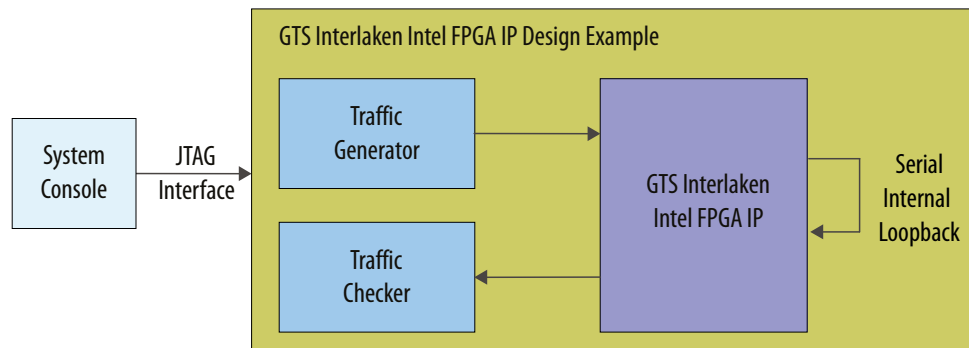
Figure 1. Development Steps for the Design Example



The F-Tile Interlaken Intel FPGA IP core design example supports the following features:

- Internal TX to RX serial loopback mode
- Automatically generates fixed size packets
- Basic packet checking capabilities
- Ability to use System Console to reset the design for re-testing purpose

Figure 2. High-level Block Diagram



Related Information

- [F-Tile Interlaken Intel FPGA IP User Guide](#)
- [F-Tile Interlaken Intel FPGA IP Release Notes](#)

1.1. Hardware and Software Requirements

To test the example design, use the following hardware and software:

以上内容仅为本文档的试下载部分，为可阅读页数的一半内容。如要下载或阅读全文，请访问：<https://d.book118.com/896121133243010210>