

SN54LVTH16245A, SN74LVTH16245B 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS143M – MAY 1992 – REVISED MARCH 2000

Members of the Texas Instruments Widebus™ Family

State-of-the-Art Advanced BiCMOS
Technology (ABT) Design for 3.3-V
Operation and Low Static-Power
Dissipation

Support Mixed-Mode Signal Operation
(5-V Input and Output Voltages With
3.3-V V_{CC})

Support Unregulated Battery Operation
Down to 2.7 V

Distributed V_{CC} and GND Pins Minimize
High-Speed Switching Noise

Flow-Through Architecture Optimizes PCB
Layout

Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$

I_{off} and Power-Up 3-State Support Hot
Insertion

Bus Hold on Data Inputs Eliminates the
Need for External Pullup/Pulldown
Resistors

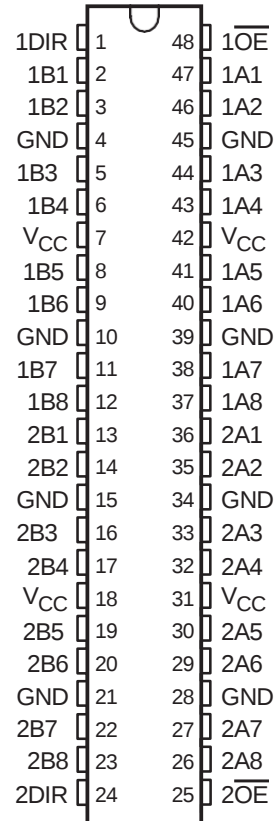
Latch-Up Performance Exceeds 100 mA Per
JESD 78, Class II (SN74LVTH16245B Only)

ESD Protection Exceeds JESD 22

- 2000-V Human-Body Model (A114-A)
- 200-V Machine Model (A115-A)
- 1000-V Charged-Device Model (C101)
(SN74LVTH16245B Only)

Package Options Include Plastic Shrink
Small-Outline (DL), Thin Shrink
Small-Outline (DGG), and Thin Very
Small-Outline (DGV) Packages and 380-mil
Fine-Pitch Ceramic Flat (WD) Package
Using 25-mil Center-to-Center Spacings

SN54LVTH16245A ... WD PACKAGE SN74LVTH16245B ... DGG, DGV, OR DL PACKAGE (TOP VIEW)



description

The SN54LVTH16245A and SN74LVTH16245B devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the devices so that the buses are effectively isolated.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II (SN74LVTH16245B Only)
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101) (SN74LVTH16245B Only)
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SN54LVTH16245A . . . WD PACKAGE
SN74LVTH16245B . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1DIR	1	48	$\overline{1OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	$\overline{2OE}$

description

The SN54LVTH16245A and SN74LVTH16245B devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the devices so that the buses are effectively isolated.



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SN54LVTH16245A, SN74LVTH16245B

3.3-V ABT 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH16245A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16245B is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN54LVTH16245A, SN74LVTH16245B

3.3-V ABT 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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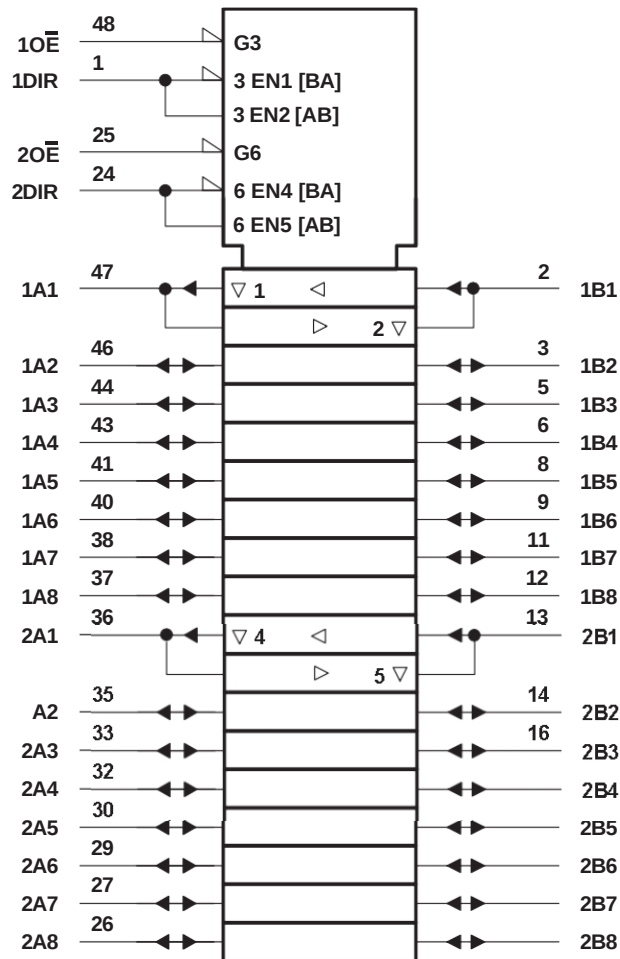
SN54LVTH16245A, SN74LVTH16245B

3.3-V ABT 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

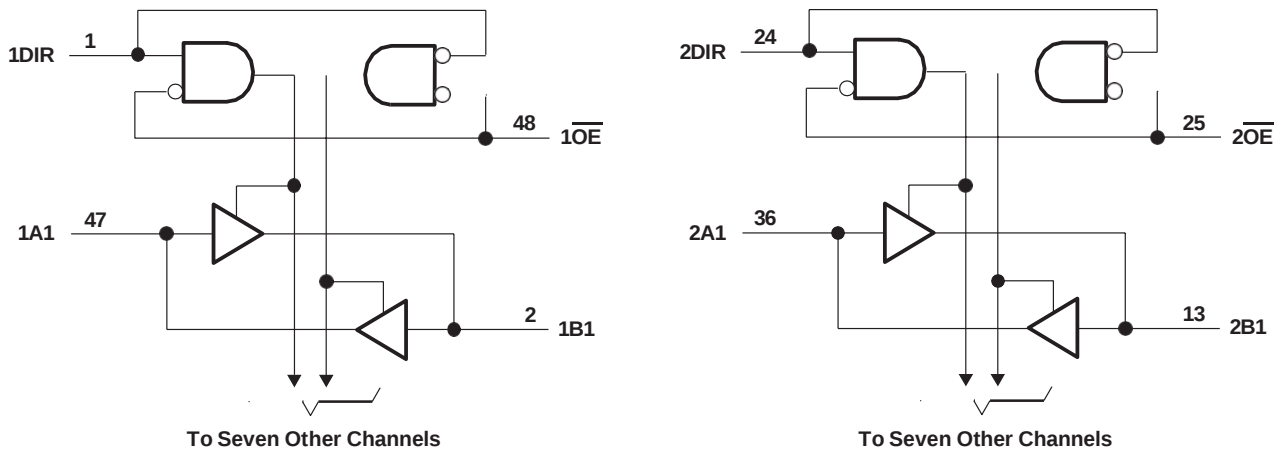
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

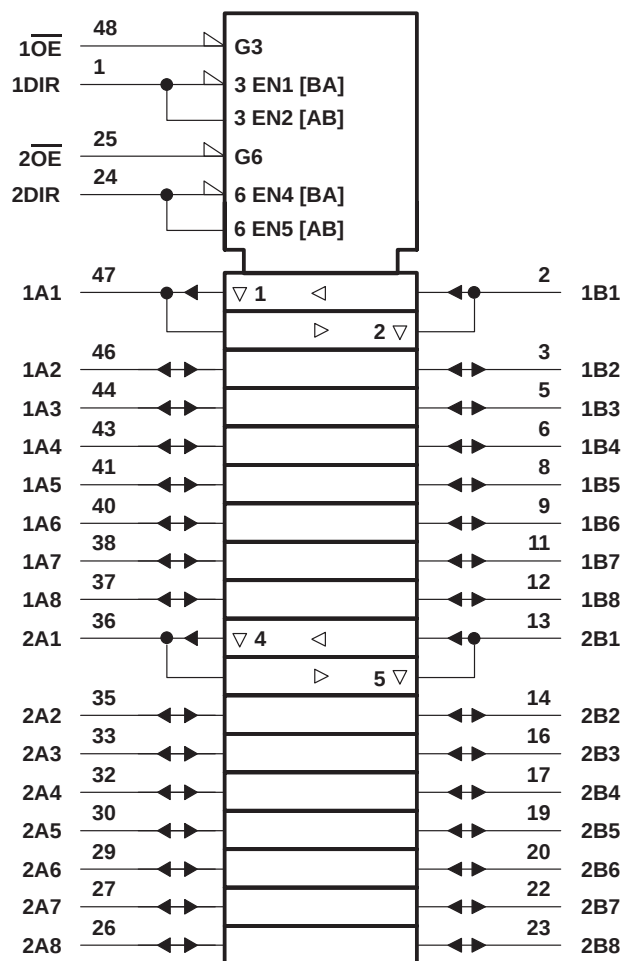
logic diagram (positive logic)



SN54LVTH16245A, SN74LVTH16245B 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

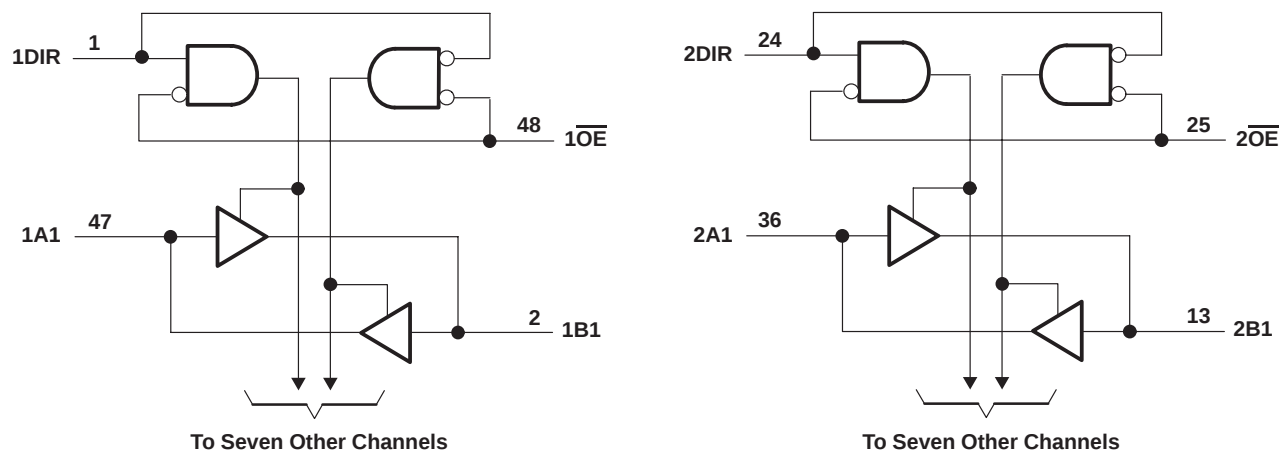
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logic diagram (positive logic)



SN54LVTH16245A, SN74LVTH16245B

3.3-V ABT 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	V to 4.6 V
Input voltage range, V_I (see Note 1)	V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16245A.....	96 mA
SN74LVTH16245B	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16245A.....	48 mA
SN74LVTH16245B	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T_{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH16245A		SN74LVTH16245B		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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3.3-V ABT 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16245A	96 mA
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recommended operating conditions (see Note 4)

		SN54LVTH16245A		SN74LVTH16245B		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

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3.3-V ABT 16-BIT BUSTRANSCEIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16245A			SN74LVTH16245B			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}		V _{CC} = 2.7 V, I _I = −18 mA		−1.2			−1.2			V	
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = −100 μA		V _{CC} −0.2			V _{CC} −0.2			V	
		V _{CC} = 2.7 V, I _{OH} = −8 mA		2.4			2.4				
		V _{CC} = 3 V	I _{OH} = −24 mA	2							
			I _{OH} = −32 mA				2				
V _{OL}		V _{CC} = 2.7 V	I _{OL} = 100 μA	0.2			0.2			V	
			I _{OL} = 24 mA	0.5			0.5				
		V _{CC} = 3 V	I _{OL} = 16 mA	0.4			0.4				
			I _{OL} = 32 mA	0.5			0.5				
			I _{OL} = 48 mA	0.55							
			I _{OL} = 64 mA				0.55				
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1			±1			μA	
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10			10				
	A or B ports‡	V _{CC} = 3.6 V	V _I = 5.5 V		20			20			
			V _I = V _{CC}		5			1			
			V _I = 0		−5			−5			
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100			μA	
I _I (hold)	A or B ports	V _{CC} = 3 V	V _I = 0.8 V		75			75			μA
			V _I = 2 V		−75			−75			
		V _{CC} = 3.6 V§, V _I = 0 to 3.6 V					±500				
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care		±100*			±100			μA	
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care		±100*			±100			μA	
I _{CC}		V _{CC} = 3. V, I _O = 0, V _I = V _{CC} or GND	Outputs high		0.19			0.19			mA
			Outputs low		5			5			
			Outputs disabled		0.19			0.19			
ΔI _{CC} ¶		V _{CC} = 3 V to 3.6, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.2			0.2			mA	
C _i		V _I = 3 V or 0		4			4			pF	
C _{io}		V _O = 3 V or 0		10			10			pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at $V_{CC}\text{ or GND}$

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

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V _{IK}		V _{CC} = 2.7 V, I _I = −18 mA		−1.2			−1.2			V	
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = −100 μA		V _{CC} −0.2			V _{CC} −0.2			V	
		V _{CC} = 2.7 V, I _{OH} = −8 mA		2.4			2.4				
		V _{CC} = 3 V	I _{OH} = −24 mA	2							
			I _{OH} = −32 mA				2				
V _{OL}		V _{CC} = 2.7 V	I _{OL} = 100 μA	0.2			0.2			V	
			I _{OL} = 24 mA	0.5			0.5				
		V _{CC} = 3 V	I _{OL} = 16 mA	0.4			0.4				
			I _{OL} = 32 mA	0.5			0.5				
			I _{OL} = 48 mA	0.55							
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I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1			±1			μA	
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10			10				
	A or B ports‡	V _{CC} = 3.6 V	V _I = 5.5 V		20			20			
			V _I = V _{CC}		5			1			
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I _I (hold)	A or B ports	V _{CC} = 3 V	V _I = 0.8 V		75			75			μA
			V _I = 2 V		−75			−75			
		V _{CC} = 3.6 V§, V _I = 0 to 3.6 V					±500				
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care		±100*			±100			μA	
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care		±100*			±100			μA	
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		0.19			0.19			mA
			Outputs low		5			5			
			Outputs disabled		0.19			0.19			
ΔI _{CC} ¶		V _{CC} = 3 V to 3.6, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.2			0.2			mA	
C _i		V _I = 3 V or 0		4			4			pF	
C _{io}		V _O = 3 V or 0		10			10			pF	

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