

Features

- Single-voltage Operation
 - 5V Read
 - 5V Reprogramming
- Fast Read Access Time - 55 ns
- Internal Program Control and Timer
- Sector Architecture
 - One 16K Byte Boot Block with Programming Lockout
 - Two 8K Byte Parameter Blocks
 - Two Main Memory Blocks (96K, 128K Bytes)
- Fast Erase Cycle Time - 10 seconds
- Byte-by-byte Programming - 10 μ s/Byte Typical
- **Hardware Data Protection**
- DATA Polling for End of Program Detection
- Low Power Dissipation
 - 50 mA Active Current
 - 100 μ A CMOS Standby Current
- Typical 10,000 Write Cycles

Description

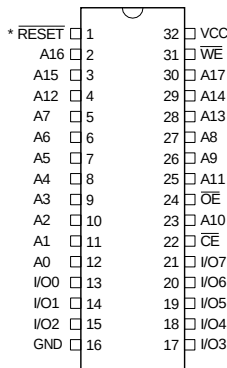
The AT49F002(N)(T) is a 5-volt only in-system reprogrammable Flash memory. Its 2 megabits of memory is organized as 262,144 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 55 ns with power dissipation of just 275 mW over the commercial temperature range.

(continued)

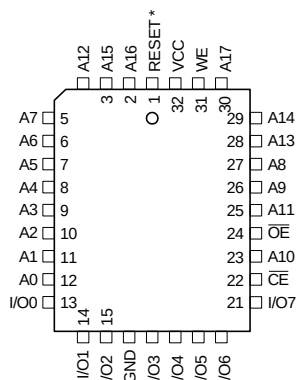
Pin Configurations

Pin Name	Function
A0 - A17	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RESET}$	RESET
I/O0 - I/O7	Data Inputs/Outputs
DC	Don't Connect

DIP Top View

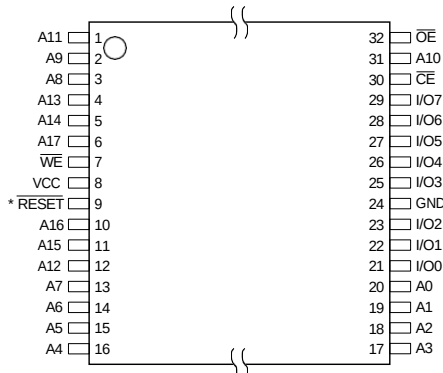


PLCC Top View



VSOP Top View (8 x 14 mm) or
TSOP Top View (8 x 20 mm)

Type 1



*Note: This pin is a DC on the AT49F002(N)(T).



**2-megabit
(256K x 8)
5-volt Only
Flash Memory**

**AT49F002
AT49F002N
AT49F002T
AT49F002NT**

Rev. 1017D-10/99



When the device is deselected, the CMOS standby current is less than 100 μ A. For the AT49F002N(T) pin 1 for the DIP and PLCC packages and pin 9 for the TSOP package are don't connect pins.

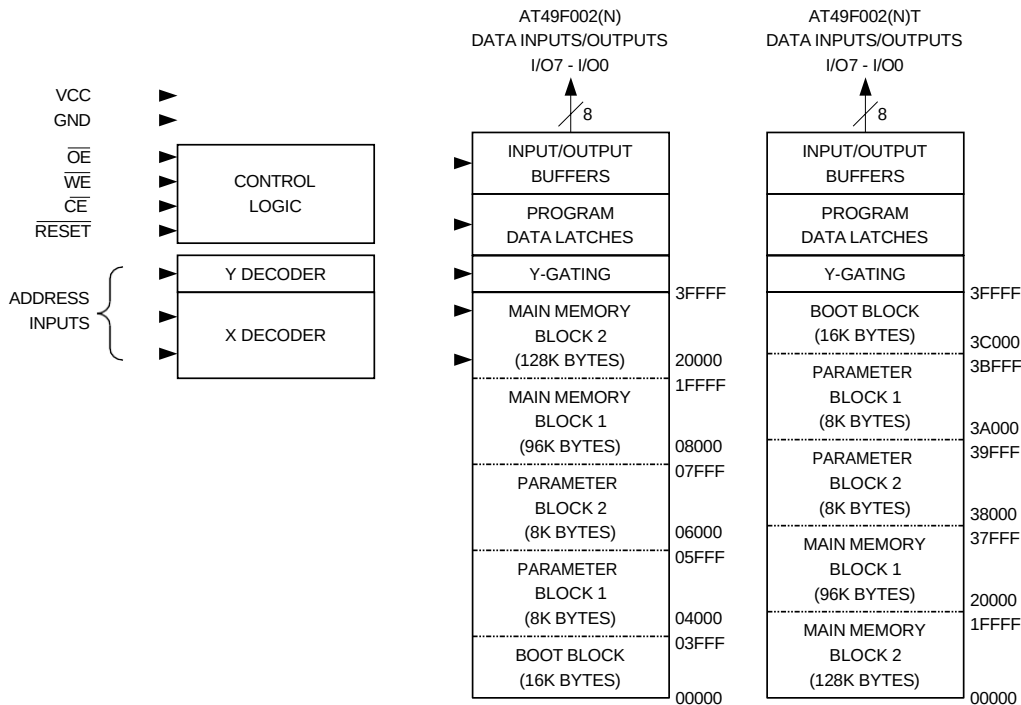
To allow for simple in-system reprogrammability, the AT49F002(N)(T) does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM; it has standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ inputs to avoid bus contention. Reprogramming the AT49F002(N)(T) is performed by erasing a block of data and then programming on a byte by byte basis. The byte programming time is a fast 50 μ s. The end of a program cycle can be optionally detected by the DATA polling feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 10,000 cycles.

The device is erased by executing the erase command sequence; the device internally controls the erase operations. There are two 8K byte parameter block sections and two main memory blocks.

The device has the capability to protect the data in the boot block; this feature is enabled by a command sequence. The 16K-byte boot block section includes a reprogramming lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is protected from being reprogrammed.

In the AT49F002(N)(T), once the boot block programming lockout feature is enabled, the contents of the boot block are permanent and cannot be changed. In the AT49F002(T), once the boot block programming lockout feature is enabled, the contents of the boot block cannot be changed with input voltage levels of 5.5 volts or less.

Block Diagram



Device Operation

READ: The AT49F002(N)(T) is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on it will be reset to the read or standby mode depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table. The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high impedance state. If the $\overline{RESET}$ pin makes a high to low transition during a program or erase operation, the operation may not be successfully completed and the operation will have to be repeated after a high level is applied to the $\overline{RESET}$ pin. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the read or standby mode, depending upon the state of the control inputs. By applying a $12V \pm 0.5V$ input signal to the $\overline{RESET}$ pin, the boot block array can be reprogrammed even if the boot block lockout feature has been enabled (see Boot Block Programming Lockout Override section). The $\overline{RESET}$ feature is not available for the AT49F002N(T).

ERASURE: Before a byte can be reprogrammed, the main memory block or parameter block which contains the byte must be erased. The erased state of the memory bits is a logical "1". The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with a specific data pattern (please refer to the Chip Erase Cycle Waveforms).

After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is t_{EC} . If the boot block lockout feature has been enabled, the data in the boot sector will not be erased.

CHIP ERASE: If the boot block lockout has been enabled, the Chip Erase function will erase Parameter Block 1, Parameter Block 2, Main Memory Block 1, and Main Memory Block 2 but not the boot block. If the Boot Block Lockout has not been enabled, the Chip Erase function will erase the entire chip. After the full chip erase the device will return back to read mode. Any command during chip erase will be ignored.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into sectors that can be individually erased. There are two 8K-byte parameter block sections and two main memory blocks. The 8K-byte parameter block sections can be independently erased and reprogrammed. The two main memory sections are designed to be used as alternative memory sectors. That is, whenever one of the blocks has been erased and reprogrammed, the other block should be erased and reprogrammed before the first block is again erased. The Sector Erase command is a six bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H data input command is latched at the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion.

BYTE PROGRAMMING: Once the memory array is erased, the device is programmed (to a logical "0") on a byte-by-byte basis. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is accomplished via the internal device command register and is a 4 bus cycle operation (please refer to the Command Definitions table). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, and the data latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Programming is completed after the specified t_{BP} cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 16K bytes. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the boot block is 00000 to 03FFF for the AT49F002(N) while the address

range of the boot block is 3C000 to 3FFFF for the AT49F002(N)T.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed with input voltage levels of 5.5V or less. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out for the AT49F002(N), and a read from address location 3C002H will show if programming the boot block is locked out for AT49F002(N)T. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been activated and the block cannot be programmed. The software product identification exit code should be used to return to standard operation.

BOOT BLOCK PROGRAMMING LOCKOUT OVERRIDE:

The user can override the boot block programming lockout by taking the RESET pin to 12 volts. By doing this, protected boot block data can be altered through a chip erase, sector erase or word programming. When the RESET pin is brought back to TTL levels the boot block programming lockout feature is again active. This feature is not available on the AT49F002N(T).

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49F002(N)(T) features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. DATA polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling the AT49F002(N)(T) provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49F002(N)(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) Program inhibit: holding any one of OE low, $\overline{\text{CE}}$ high or WE high inhibits program cycles. (c) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

Command Definition (in Hex)⁽¹⁾

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D _{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA ⁽⁴⁾	30
Byte Program	4	5555	AA	2AAA	55	5555	A0	Addr	D _{IN}				
Boot Block Lockout ⁽²⁾	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit ⁽³⁾	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit ⁽³⁾	1	XXXX	F0										

- Notes:
- The DATA FORMAT in each bus cycle is as follows: I/O7 - I/O0 (Hex)
 - The 16K byte boot sector has the address range 00000H to 03FFFH for the AT49F002(N) and 3C000H to 3FFFFH for the AT49F002(N)T
 - Either one of the Product ID Exit commands can be used.
 - SA = sector addresses:
 For the AT49F002(N):
 SA = 00000 to 03FFF for BOOT BLOCK
 Nothing will happen and the device goes back to the read mode in 100 ns
 SA = 04000 to 05FFF for PARAMETER BLOCK 1
 SA = 06000 to 07FFF for PARAMETER BLOCK 2
 SA = 08000 to 1FFFF for MAIN MEMORY ARRAY BLOCK 1
 This command will erase - PB1, PB2 and MMB1
 SA = 20000 to 3FFFF for MAIN MEMORY ARRAY BLOCK 2

 For the AT49F002(N)T:
 SA = 3C000 to 3FFFF for BOOT BLOCK
 Nothing will happen and the device goes back to the read mode in 100 ns
 SA = 3A000 to 3BFFF for PARAMETER BLOCK 1
 SA = 38000 to 39FFF for PARAMETER BLOCK 2
 SA = 20000 to 37FFF for MAIN MEMORY ARRAY BLOCK 1
 This command will erase - PB1, PB2 and MMB1
 SA = 00000 to 1FFFF for MAIN MEMORY ARRAY BLOCK 2

Absolute Maximum Ratings*

Temperature Under Bias.....	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground.....	V to +6.25V
All Output Voltages with Respect to Ground.....	V to V _{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground.....	V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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