Serial Lite III Streaming Stratix® 10 FPGA IP Design Example User Guide

Updated for Quartus® Prime Design Suite: **24.1**

IP Version: **20.1.0**

Online Version
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683341
UG-20065
2024.05.23

Contents

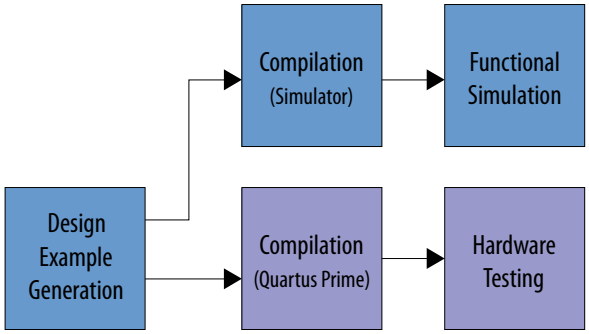
1. Quick Start Guide

The Serial Lite III Streaming Intel® FPGA IP provides the capability of generating design examples for selected configurations.

The Serial Lite III Streaming Intel FPGA IP offers eight preset settings for Stratix® 10 H-tile and L-tile devices in both simplex and duplex modes and Stratix 10 E-tile devices in duplex mode.

- Standard Clocking Mode 6x12.5G
- Standard Clocking Mode 6x17.4G
- Standard Clocking Mode 2x25G
- Standard Clocking Mode 4x28G
- Advanced Clocking Mode 6x12.5G
- Advanced Clocking Mode 6x17.4G
- Advanced Clocking Mode 2x25G
- Advanced Clocking Mode 4x28G

Figure 1. Development Stages for the Design Example



Related Information

- Serial Lite III Knowledge Base
- Serial Lite III Streaming Intel FPGA IP User Guide
- Serial Lite III Streaming Intel FPGA IP Core Release Notes

1.1. Directory Structure

The Quartus® Prime software generates the design example files in the following folders:

- <user_defined_design_example_directory>/ed_sim
- <user_defined_design_example_directory>/ed_synth
- <user_defined_design_example_directory>/ed_hwtest

The following diagrams show the directories that contain the generated files for the design examples.

Figure 2. Directory Structure for Stratix 10 Serial Lite III Streaming Design Example

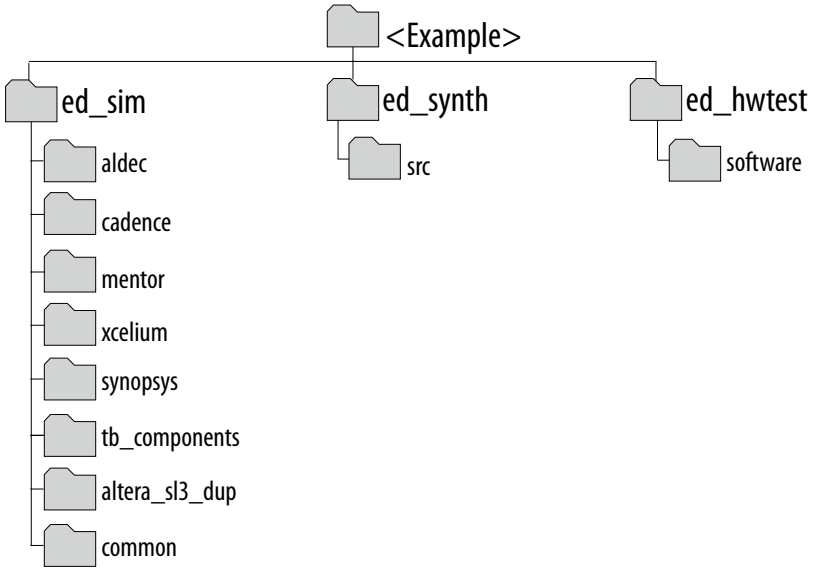


Table 1. Directory and File Description for Design Example Folder

Directory/File	Description
ed_sim/tb_components	The folder that contains the testbench files.
ed_sim/common	The folder that contains the .tcl scripts for all the simulators.
ed_sim/cadence ed_sim/aldec ed_sim/mentor ed_sim/xcelium ed_sim/synopsys/vcs or ed_sim/synopsys/vcsmx	The folder that contains the simulation script. It also serves as a working area for the simulator.
ed_sim/altera_sl3_dup	The folder that contains the design example simulation source files.
ed_synth/seriallite_iii_streaming_demo.qpf	Quartus project file.
ed_synth/seriallite_iii_streaming_demo.qsf	Quartus settings file.
ed_synth/seriallite_iii_streaming_demo.sdc	Synopsys Design Constraints (SDC) file.
ed_synth/src	The folder that contains the design example synthesizable components.
ed_synth/src/seriallite_iii_streaming_demo.v	Design example top-level HDL.

continued...

Directory/File	Description
ed_synth/altera_sl3_dup/synth/altera_sl3_dup.v	Design example DUT top-level files.
ed_synth/demo_control	The folder for each synthesizable component including Platform Designer generated IPs, such as demo_mgmt and demo_control.
ed_hwtest	The folder that contains the design example hardware setup files.
ed_hwtest/Readme.txt	Instruction file to download the generated design example on the development kit.
ed_hwtest/master_export.v	User interface Verilog design file. This file is available when you instantiate a design with Synthesis enabled.
ed_hwtest/master_export_hw.tcl	Component description file for master export custom IP. This file is available when you instantiate a design with Synthesis enabled.
ed_hwtest/software	The folder that contains scripts to download the demo_control program into Nios® V processor and open an interactive terminal to run the design example.

1.2. Design Example Block Diagrams

Figure 3. High-Level Block Diagram for Stratix 10 H-tile and L-tile Design Examples

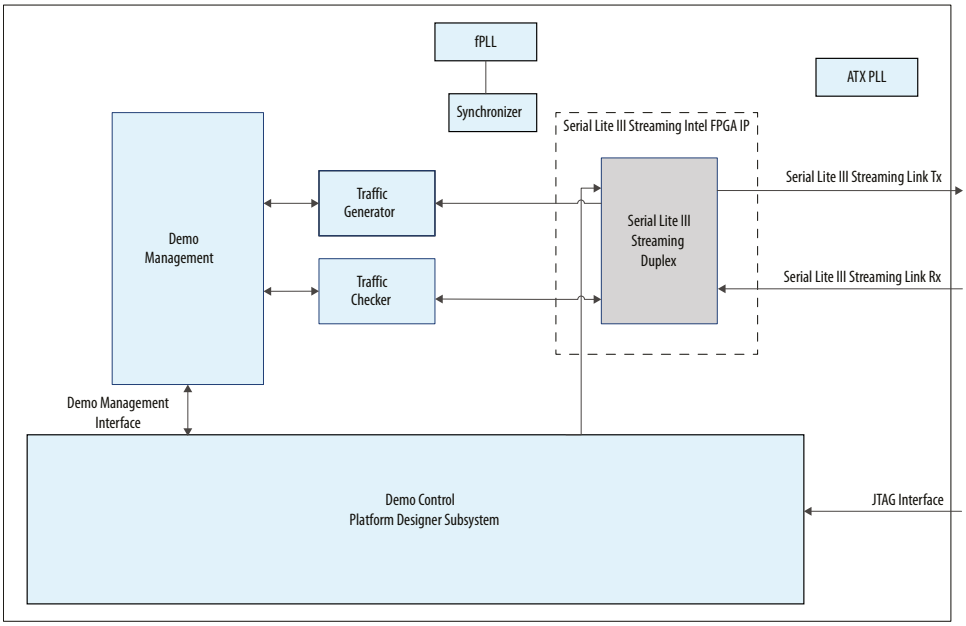
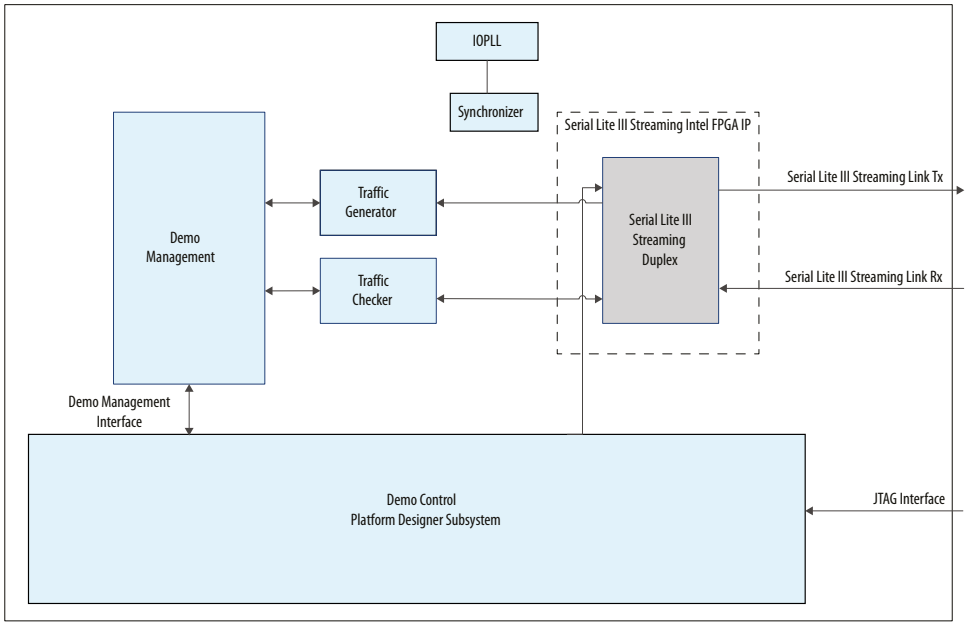


Figure 4. High-Level Block Diagram for Stratix 10 E-tile Design Examples



1.3. Generating the Design

You can use the Serial Lite III Streaming IP core parameter editor in the Quartus Prime software to generate the design example.

Figure 5. Procedure

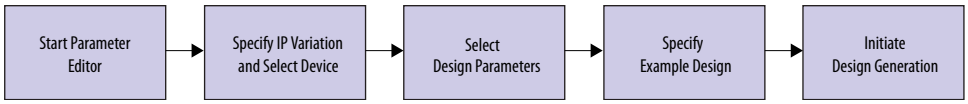
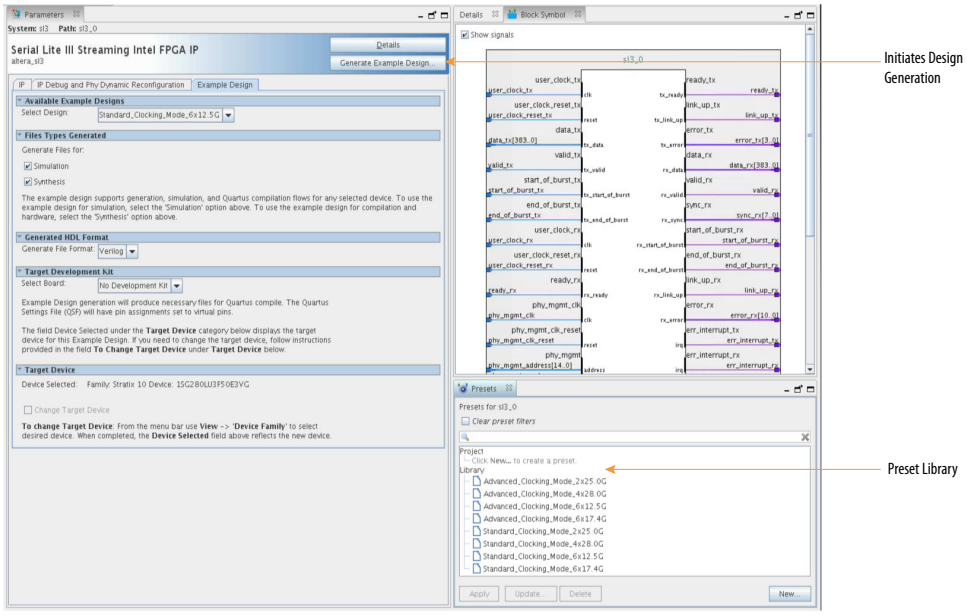


Figure 6. Example Design Tab



1.3.1. Procedure

This is a general procedure on how to generate the design example.

To generate the design example from the IP parameter editor:

1. In the IP Catalog (`Tools > IP Catalog`), locate and select **Serial Lite III Streaming**. The IP parameter editor appears.
2. Specify a top-level name and the folder for your custom IP variation. Click **OK**.
3. Select a design from the **Presets** library and click **Apply**. When you select a design, the system automatically populates the IP parameters for the design.

   Note: If you select another design, the settings of the IP parameters change accordingly.
4. Specify the parameters for your design.
5. Click the **Generate Example Design** button.

The software generates all design files in the sub-directories. These files are required to run simulation, compilation, and hardware testing.

1.3.2. Design Example Parameters

The Serial Lite III Streaming IP parameter editor includes an *Example Design* tab for you to specify certain parameters before generating the design example.

Table 2. Parameters in the Example Design Tab

Parameter	Description
Select Design	Available example designs for the IP parameter settings. When you select a design from the Preset library, this field shows the selected design.
Generate Files for	The files to generate for different development phases. Simulation—when selected, the necessary files for simulating the design example are generated. Synthesis—when selected, the synthesis files are generated. Use these files to compile the design in the Quartus Prime software for hardware testing.
Generate File Format	The format of the RTL files for simulation—Verilog or VHDL.
Select Board	Supported hardware for design implementation. When you select an Intel FPGA development board, the *Target Device* is the one that matches the device on the Development Kit. If this menu is grayed out, there is no supported board for the options that you select. **Stratix 10 GX Signal Integrity Development Kit:** This option allows you to test the design example on selected Intel FPGA IP development kit. This selection automatically selects the *Target Device* to match the device on the Intel FPGA IP development kit. If your board revision has a different speed grade, you can change the target device. **Custom Development Kit:** This option allows you to test the design example on a third party development kit with Intel FPGA IP device, a custom designed board with Intel FPGA IP device, or a standard Intel FPGA IP development kit not available for selection. You can also select a custom device for the custom development kit. **No Development Kit**: This option excludes the hardware aspects for the design example.
Change Target Device	Select a different device grade for Intel FPGA IP development kit. For device-specific details, refer to the device datasheet on the Intel FPGA website.

1.3.3. Presets

Standard presets allow instant entry of pre-selected parameter values in the **IP** and **Example Design** tabs. You can select the presets at the lower right window in the parameter editor.

The parameter values chosen for the presets belong to the group of supported Serial Lite III Streaming IP configurations for design example generation. You can select one of the presets available for your target device to quickly generate a design example without having to manually set each parameter in the **IP** tab and verifying that the parameter matches the supported configurations set. There are eight preset settings available in the library that support Duplex, Sink and Source modes:

- Standard Clocking Mode 6x12.5G
- Standard Clocking Mode 6x17.4G
- Standard Clocking Mode 2x25G
- Standard Clocking Mode 4x28G
- Advanced Clocking Mode 6x12.5G
- Advanced Clocking Mode 6x17.4G
- Advanced Clocking Mode 2x25G
- Advanced Clocking Mode 4x28G

Note: Serial Lite III Streaming Intel FPGA IP design examples for Stratix 10 devices are only available in Quartus Prime Pro Edition.

Table 3. Parameter Settings for Stratix 10 Design Example Standard Clocking Presets

Presets	Standard Clocking Mode 6x12.5G	Standard Clocking Mode 6x17.4G	Standard Clocking Mode 2x25G	Standard Clocking Mode 4x28G
Direction	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)
Number of lanes	6	6	2	4
Meta frame length in words	200	200	200	200
Transceiver reference clock frequency (MHz)	312.5	600.0	312.5	200.0
Enable M20K ECC support	ON/OFF The default value is OFF.	ON/OFF The default value is OFF.	ON/OFF The default value is OFF.	ON/OFF The default value is OFF.
Clocking Mode	Standard clocking mode	Standard clocking mode	Standard clocking mode	Standard clocking mode
Required user clock frequency (MHz)	177.556818	247.159091	355.113636	397.727273
Transceiver data rate (Gbps)	12.5	17.4	25.0	28.0
Streaming Mode	Full	Full	Full	Full
VCCR_GXB and VCCT_GXB supply voltage for the transceiver	1.0 V (applicable only for L-tile and H-tile devices)	1.0 V (applicable only for L-tile and H-tile devices)	1.1 (applicable only for L-tile and H-tile devices)	1.1 (applicable only for L-tile and H-tile devices)
Transceiver Channel Type	GX (applicable only for L-tile and H-tile devices)	GX (applicable only for L-tile and H-tile devices)	GXT (applicable only for L-tile and H-tile devices)	GXT (applicable only for L-tile and H-tile devices)
Transceiver Tile	L-tile, H-tile, and E-tile devices	L-tile, H-tile, and E-tile devices	L-tile, H-tile, and E-tile devices	L-tile, H-tile, and E-tile devices

Table 4. Parameter Settings for Stratix 10 Design Example Advanced Clocking Presets

Presets	Advanced Clocking Mode 6x12.5G	Advanced Clocking Mode 6x17.4G	Advanced Clocking Mode 2x25G	Advanced Clocking Mode 4x28G
Direction	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)	• Simplex and Duplex (H-tile and L-tile) • Duplex (E-tile)
Number of lanes	6	6	2	4
Meta frame length in words	200	200	200	200
Transceiver reference clock frequency (MHz)	312.5	600.0	312.5	200.0
Enable M20K ECC support	ON/OFF	ON/OFF	ON/OFF	ON/OFF

continued...