1 Revision History

Revision History

Version	Date	Comment
0.1	2013-06-06	Preliminary

2 INTRODUCTION

This specification provides a convenient reference for those who work on product development; it provides a general overview and points out the unique aspects of B400G3 without duplicating information available in component specifications. Information contained within this document includes a product outline and a brief summary of each subsystem.

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2.1 Summary of System Features

B400G3 is the Multi-server products targeted for announcement with Intel Denlow platform in 2012. B400G3 will utilize the same Performance Intel, PCA, but include two different entry level platforms with variations in chassis height (1U vs. 2U).

Intel Denlow platform consists of the Haswell-DT processor, the Platform Controller Hub (Intel®C222/C224/C226 chipset).

Table 1 Summary of Performance Intel, B400G3 PCA Features

Item Name	Description
Processors	• 1P Haswell-DT CPU with integrated memory controller
Chipset	• Intel®Lynx point chipset
MEMORY	• DDR3 1333/1600 UDIMM ECC • 2 channels • Up to 2 UDIMMs per channel
System Management	• Embedded NIC dedicated for Management
VGA	• ASPEED AST1300 • 1 rear VGA connector
Networking	• 1x Intel I210 GbE Controller • 3x Intel I211 GbE Controller
USB2.0	• PCH controller • 2 front, 2 inner, 4 rear USB connectors
Onboard Slots	• One PCI-E x16(x8 lane) Gen3 Interface Slot2 • One PCI-E x16(x8 lane) Gen3 Interface Slot6
Onboard Storage port	• 2 SATA 6Gb/s ports, 4 SATA 3Gb/s ports （C222） • 6SATA 6Gb/s ports(PCIE→SATA)

Table 1 Summary of Performance Intel, B400G3 PCA Features

Item Name	Description
DVD	• **Optional DVD (SATA)**
BIOS ROM	• **SPI Flash for PCH**
COM Port	• **One Serial Port from AST1300**
Fan control	• **PWM fan speed control** • **9 Fan connectors(CPU Fan and Fan1 is just using the same PWM signal)**

2.2 Reference Documents

The following table lists the specification revision that would be referred to B400G3.

Table 2 Documentation References

Document Name	Revision	Document Source
DenlowServer Platform Design Guide (PDG)	**Version2.0**	**Intel Confidential**
Lynx Point Platform Controller Hub (PCH) External Design Specification (EDS)	**Version 1.5**	**Intel Confidential**
Sugar Bay and Denlow-WS Platform Design Guide (PDG)	**Version 1.5**	Intel Confidential
DenlowServer Customer Reference Board (CRB)	**Version V1.4**	Intel Confidential
HaswellProcessor - Desktop UP Server/ Workstation and Mobile Platforms External Design Specification (EDS)	**Version 1.5**	Intel Confidential

2.3 Terminology

Table 3 General Terminology

Terminology	Description
Channel	In the IMC(Integrated Memory Controller), a DDR3 channel is the set of signals that connects to one set of DDR3 DIMMs. The IMC of Gainstown has up to three DDR3 channels.
CSI	Common System Interface, Intel developed, cache-coherent, link-based interconnect specification. See also Intel® QuickPath interconnect.
DDR	Double Data Rate SDRAM. DDR describes the type of DRAMs that transfers two data items per clock on each pin. This is the only type of DRAM supported by the IMC.
DDR3	Native Double Data Rate 3 memory technology.
DIMM	Dual-in-Line Memory Module. A packaging arrangement of memory devices on a socketable substrate.
ESI	Enterprise Southbridge Interface.
ESS	Enterprise Storage and Servers
FWH	Firmware Hub, it is actually a flash memory with the LPC interface.
LFF	Large Form Factor
GB/s	Gigabytes per second (1000 Mbytes per second).
Gb/s	Gigabits per second (1000 Mbits per second).
PCH	Platform Controller Hub
IMC	Integrated Memory Controller.
Intel® QuickPath interconnect	Intel developed, cache-coherent, link-based interconnect specification. See also CSI.
IPMI	Intelligent Platform Management Interface.
RAID	Redundant Array of Independent Disks. RAID improves performance by disk striping, which interleaves bytes or groups of bytes across multiple drives, so more than one disk is reading and writing simultaneously.
SATA	Serial ATA.
SFF	Small Form Factor
SMBus	System Management Bus. Mastered by a system management controller to read and write configuration registers. Signaling and protocol are loosely based on I2C*, limited to 100 KHz.
UHCI	Universal Host Controller Interface.
USB	Universal Serial Bus.

Table 3 General Terminology

Terminology	Description
VID	Voltage Identification (VID) is a group of input bits into a voltage regulator to set the output voltage.

3 MLB Overview

3.1 Board Code Names and Descriptions

B400G3 code name description		
Item code name	**Part Number**	**Description**
B400G3 MLB	**6050A**	**B400G3 mother board**

3.2 Platform Overview

3.2.1 Summary of B400G3 Product Definition

- **Key Features**
  - **1P Intel Highly integrated one-chip solution Haswell-DT Processor, Intel®Lynx point** chipset
  - **Integrated DDR3 memory controller & PCI-E**
  - **Up to 16 lanes from CPU, 8 lanes from PCH**
- **Memory**
  - **DDR3 1333/1600 UDIMM ECC**
  - **2 channels**
  - **Up to 2 UDIMMs per channel**
  - **32GB max at launch with UDIMMs (2Gb DRAM)**
- **Storage**
  - **2xSATA 6Gb/s ports(PCH), 4xSATA 3Gb/s ports(PCH), 6SATA 6Gb/s ports(ASM1061, option)**

- **BMC**
  - **Aspeed 1300**
  - **Integrated VGA**
- **Networking**
  - **Intel one port 1Gbe NIC controller I210, and Intel one port 1Gbe NIC controller I211**
  - **Integrated 10/100M management NIC PORT(BCM5221 PHY required, option)**
- **Media Bays and Ports**
  - **USB 2.0 front (2), inner(2 option) and rear (4)**
  - **Serial port**
  - **Video**
  - **Four port 1GbE NIC**
- **Power Supply**

（TBD）

- **I/O Config Options**
  - **TBD**

3.3 Mother Board Placement

The layout of Mother Board is shown as below. Each connector and major component is identified by number.

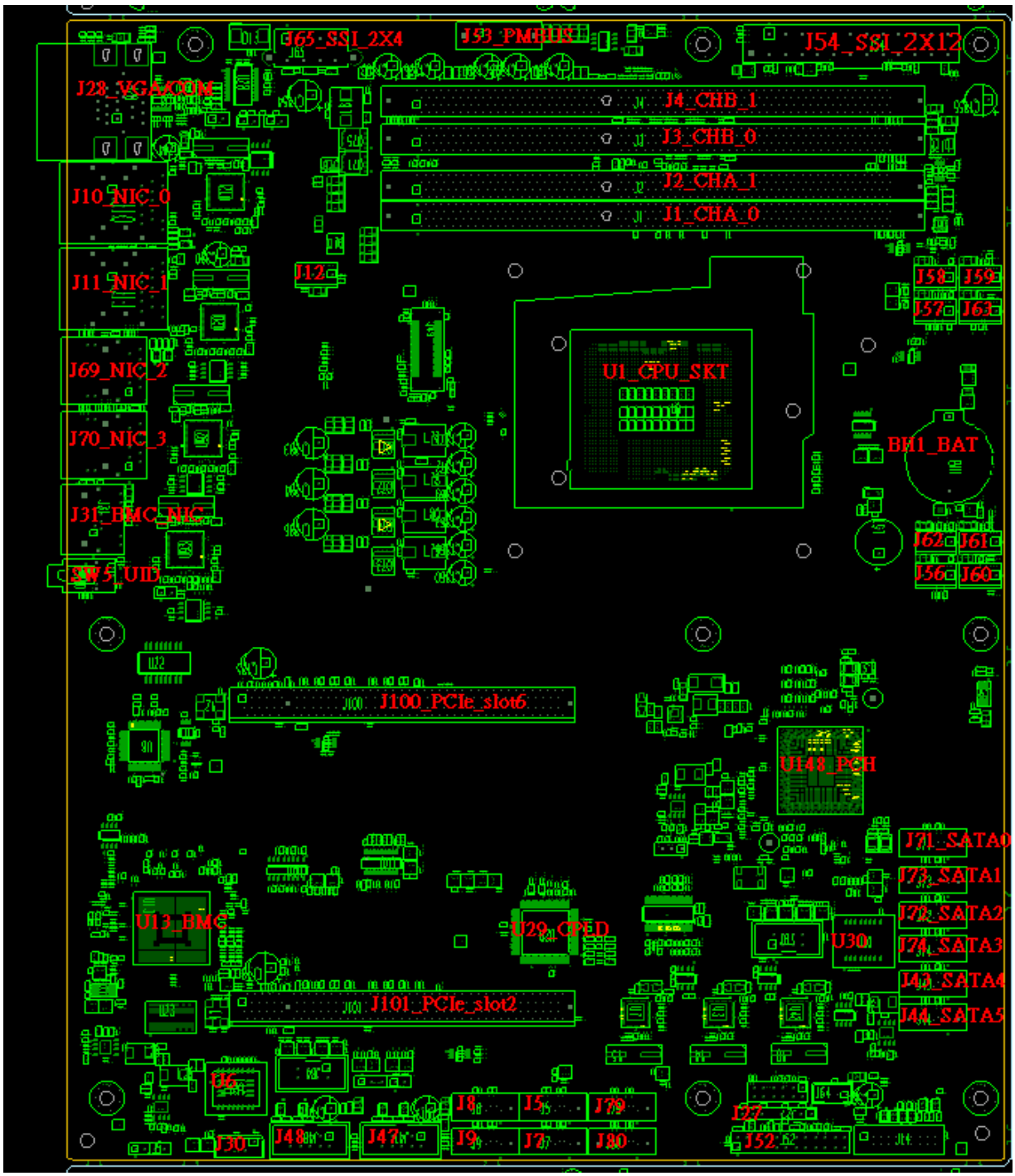

Figure .1 Placements on Motherboard

Table 4 B400G3 Components Versus Placement Relation

Location	**Description**	Location	Description
J65	2x4_SSI_power_conn	J53	PM_BUS_CONN
J54	2x14_SSI_power_conn	J4	DIMM_slot_CHB_1
J28	VGA/COM_CONN	J3	DIMM_slot_CHB_0
J10	NIC0_CONN	J2	DIMM_slot_CHA_1
J11	NIC1_CONN	J1	DIMM_slot_CHA_0
J69	NIC2_CONN	J100	PCIe_slot6
J70	NIC3_CONN	J101	PCIe_slot2
J31	BMC_NIC	U13	BMC
SW5	UID_LED/BTN	U29	CPLD
U1	CPU_SOCKET	U148	PCH
BH1	Battery	U30	BIOS_FLASH
J58	FAN_CONN1	U6	BMC_FLASH
J59	FAN_CONN2	J30	IPMB_CONN
J57	FAN_CONN3	J48	INT_USB_CONN1
J63	FAN_CONN4	J47	INT_USB_CONN2
J62	FAN_CONN5	J27	CPLD_JTAG_CONN
J61	FAN_CONN6	J52	FP_CONN
J56	FAN_CONN7	J71	SATA0_CONN
J60	FAN_CONN8	J73	SATA1_CONN
J12	CPU_FAN	J72	SATA2_CONN
J43	SATA4_CONN	J74	SATA3_CONN
J44	SATA5_CONN	J79	SATA6_CONN
J80	SATA7_CONN	J5	SATA8_CONN
J7	SATA9_CONN	J8	SATA10_CONN
J9	SATA11_CONN		

3.4 MLB Connectors PIN definition

- **Front panel connector**

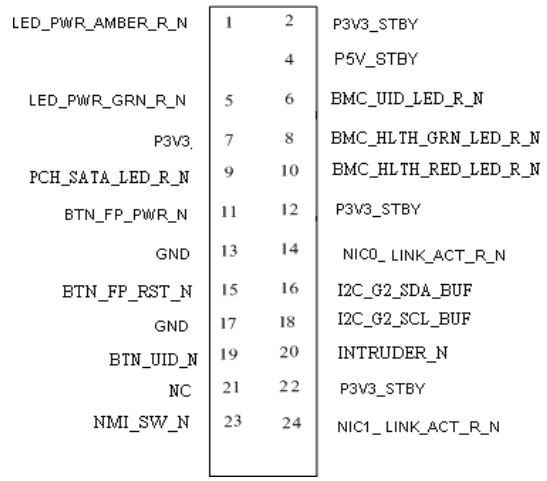

Figure.2 Front Panel Connector

Table 5 Front Panel Connector

Pin	Define	Function	Pin	Define	Function
1	LED_PWR_AMBER_R_N	Front Panel power LED	2	P3V3_STBY	Power
3	KEY		4	P5V_STBY	power
5	LED_PWR_GRN_R_N	Front Panel power LED	6	BMC_UID_BUF_R_N	UID LED
7	P3V3	power	8	BMC__HLTH_GRN_LED_R_N	Front Panel HEALTH LED
9	PCH_SATA_LED_R_N	LED for PCH	10	BMC_HLTH_RED_ LED _R_N	Front Panel HEALTH LED
11	BTN_FP_PWR_N	Power button	12	P3V3_STBY	power
13	GND	GND	14	NIC0_LINK_ACT_R_N	Activity LED for 1st NIC
15	BNT_FP_RST_N	RST button	16	I2C_G2_SDA_BUF	I2C Data to front panel thermal sensor
17	GND	GND	18	I2C_G2_SCL_BUF	I2C Clock to front panel thermal sensor
19	BMC_UID _N	UID button	20	INTRUDER_N	intruder
21	NC		22	P3V3_STBY	POWER
23	NMI_SW_N	NMI button	24	NIC1_LINK_ACT_R_N	Activity LED for 2nd NIC

- **IPMB connector**

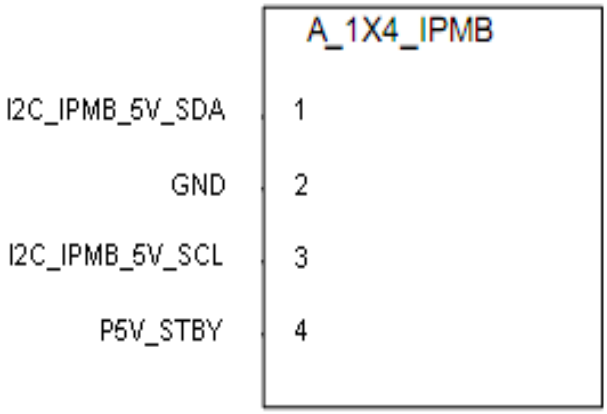

Figure.3 IPMB Connector

Table 6 IPMB Connector

Pin	Define	Function	Pin	Define	Function
1	I2C_IPMB_5V_SDA	Data of I2C bus for IPMB	3	I2C_IPMB_5V_SCL	Clock of I2C bus for IPMB
2	GND	Ground	4	P5V_STBY	P5V Standby