ESD Association Standard

ANSI/ESD S5.3.1-2009

ANSI/ESD S5.3.1-2009

Revision and Redesignation of ANSI/ESD STM5.3.1-1999

For Electrostatic Discharge Sensitivity Testing –

Charged Device Model (CDM) – Component Level

Electrostatic Discharge Association
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Rome, NY 13440

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ESD Association Standard for Electrostatic Discharge Sensitivity Testing –

Charged Device Model (CDM) – Component Level

Approved July 31, 2009
ESD Association

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FOREWORD

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a component and discharging through the component. However, with the increasing use of automated component handling systems another potentially destructive discharge mechanism, the charged device model (CDM) becomes increasingly important. In the CDM a component itself becomes charged (e.g., by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object.

Accurately quantifying the CDM discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the component will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS components for the CDM model is dielectric damage, although other damage has been noted.

The CDM sensitivity of a given component is package dependent. An integrated circuit (IC) chip in a small outline package (SOP) configuration may be more susceptible to CDM damage when compared to a dual-in-line (DIL) package configuration. ICs in thin, small outline packages (TSOP), or pin grid array (PGA) packages typically have the lowest CDM withstand voltage.

Based on results obtained with early CDM testers (not necessarily meeting the waveform requirements of this standard), components with CDM sensitivities of 500 volts or less proved difficult to handle without damage. Components with CDM sensitivities of 1,000 volts or more did not experience major field problems when proper handling techniques were followed. Recent data indicate with proper ESD controls, safe handling of devices with CDM sensitivities of 250V is achieved.

Waveform parameters for the 30 pF verification module may be subject to change in future revisions of this document.

This CDM document does not apply to the socketed discharge model testers.

This document was originally designated ANSI/ESD STM5.3.1-1999 and approved on September 26, 1999. This standard[1] is a revision of ANSI/ESD STM5.3.1-1999 and was approved on July 31, 2009. This standard was prepared by the 5.3.1 (CDM) Device Testing Subcommittee.

[1] ESD Association Standard (S): A precise statement of a set of requirements to be satisfied by a material, product, system or process that also specifies the procedures for determining whether each of the requirements is satisfied.

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ESD Association Standard for Electrostatic Discharge (ESD) Sensitivity Testing – Charged Device Model (CDM) – Component Level

1.0 SCOPE AND PURPOSE

1.1 Scope

This standard establishes the procedure for testing, evaluating and classifying the electrostatic discharge (ESD) sensitivity of components to the defined charged device model (CDM).

1.2 Purpose

The purpose of this document is to establish a test method that simulates CDM failures and provides reliable and repeatable results from tester to tester. This will allow accurate comparisons of component CDM ESD sensitivity levels.

2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0. ESD Association Glossary of Terms[2]

3.0 DEFINITIONS

The following definitions are in addition to those found in the ESD Association's Glossary of Terms:

Charged Device Model (CDM) Electrostatic Discharge (ESD). An ESD stress model that approximates the discharge event that occurs when a charged component is quickly discharged to another object at a lower electrostatic potential through a signal pin or terminal.

Charged Device Model (CDM) Electrostatic Discharge (ESD) Tester. Equipment (referred to as "tester" in this standard) that simulates the component level CDM ESD event using the non-socketed test method.

Coaxial Resistive Probe. A resistor (for example, a 1.0 ohm disk resistor) used to measure the CDM discharge current.

Field Plate (FP). A conductive plate used to elevate the potential of the device under test (DUT) by capacitive coupling (see Figure 1).

Ground Plane (GP). A conductive plate used to complete the circuitry for grounding / discharging the DUT (see Figure 1).

Non-contact Mode Discharge. An air discharge ESD event that is initiated by a probe tip or pogo pin approaching a component pin.

4.0 PERSONNEL SAFETY

The procedures and equipment described in this document may expose personnel to hazardous electrical conditions. Users of this document are responsible for selecting equipment that complies with applicable laws, regulatory codes and both external and internal policy. Users are cautioned that this document cannot replace or supersede any requirements for personnel safety.

Ground fault circuit interrupters (GFCI) and other safety protection should be considered wherever personnel might come into contact with electrical sources.

Electrical hazard reduction practices should be exercised and proper grounding instructions for equipment shall be followed.

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[2] ESD Association, 7900 Turin Road, Bldg. 3, Rome, NY 13440-2069; 315-339-6937; FAX: 315-339-6793; www.esda.org

5.0 ESD COMPONENT CLASSIFICATIONS

ESD sensitive (ESDS) components are classified according to their ESD withstand voltage using the test procedure described in this standard. The CDM ESDS component classification levels are presented in Table 1.

Table 1. CDM ESDS Component Classification Levels

Class	Voltage Range
C1	< 125 volts
C2	125 to < 250 volts
C3	250 to < 500 volts
C4	500 to < 1,000 volts
C5	1,000 to < 1,500 volts
C6	1,500 to < 2,000 volts
C7	≥ 2,000 volts

NOTE: Use the "C" prefix to indicate a CDM classification.
NOTE: For voltages above 1,500 Volts, depending on geometry of the device package, corona effects may limit the actual pre-discharge voltage and discharge current.

6.0 COMPONENT CHARGING AND DISCHARGING METHODS

Either of the following two methods may be used to raise the component potential for the subsequent CDM discharge:

6.1 Direct Charging Method

The component to be tested is placed on the field plate (FP) and charged through the pin which best provides an ohmic connection to the substrate or bulk material of the component, or through all pins simultaneously. The total charging resistance (see Figure 1) shall be at least 100 megohm. Contact to the charging pin(s) shall be established before the voltage is raised. Each pin is discharged one at a time (including power supply pins and ground pins), except the pins connected to the substrate. Re-charge the component after each pin has been discharged.

To prevent component damage, precautions shall be taken to ensure the charging mechanism and component are at ground potential prior to the initial connection. At least one megohm of the charging resistance shall be physically placed close to the charging pin to isolate the effect of any residual charge on the charge up line. It is permissible to leave the charging probe on the charging pin during the discharge cycle, provided the waveform requirements of Section 8.0 are satisfied.

NOTE: The substrate, or bulk material, is typically called Vss, or ground, for NMOS or for n-well (p-substrate) CMOS technologies; and Vcc, or Vdd, for p-well (n-substrate) CMOS technologies. For a charge-pumped substrate (where there is no direct access through an external pin), the Vss or ground pin is still appropriate to use.

6.1.1 Multichip modules or other special components (e.g., silicon-on-sapphire, silicon-on-insulator, and hybrids) shall be charged through a common power supply pin to ensure the entire component reaches the charging potential.

NOTE: For multichip modules with no common supply pin, the direct charging method is not recommended.

6.1.2 If the process technology is unknown, charge the component through the Vss or ground pin. Make note of the charging pins when reporting the results. Vpp pins shall never be used as charging pins.

6.1.3 The Dielectric layer is a non-conductive or insulative material used to form a capacitive circuit between the Field Plate (FP) and the Device Under Test (DUT). The dielectric is specifically useful for CDM when stress testing devices with metallic heat sinks. See Section 6.2 and Section 7.0, Figure 1.

6.2 Field-induced Charging Method

Place the component to be tested on the FP. Raise the potential of the component by raising the potential of the FP. Discharge through one pin. Repeat the procedure until all pins are stressed (including all power supply pins: Vdd, Vcc, Vss, Vpp, etc.).

6.2.1 The size of the FP (at least seven times larger in area than the size of the component under test) shall be such that the waveform qualification meets the requirement of Section 8.0. The FP should be connected to the power supply or ground through a greater than 100 megohm resistor (see Figure 1).

6.2.2 The size of the ground plane (GP) shall be such that it completely covers the entire device during stress testing of any of the pins, with a size margin to allow for fringing fields.

6.2.3 The thickness of the dielectric layer covering the FP shall have a maximum thickness of 130 microns (micrometers), as the presence of the dielectric reduces the package capacitance between the component and the FP, which affects the discharge current. Take precautions to ensure components are not charged prior to testing.

6.3 Discharging Method

See Informative Annex A for background information on the discharging method (non-contact mode discharge).

7.0 REQUIRED EQUIPMENT

7.1 CDM ESD Tester

Figure 1 represents the conceptual schematic for test setup to conduct field-induced CDM ESD testing. The CDM ESD tester used within the context of this standard shall meet the waveform characteristics specified in Figures 4 and 5, and Tables 3 and 4. K1 is the switch between charging the FP and grounding the FP.

NOTE: When constructing the test equipment, the parasitics in the charge and discharge paths should be minimized, since the resistance inductance-capacitance (RLC) parasitics in the equipment greatly influence the test results.

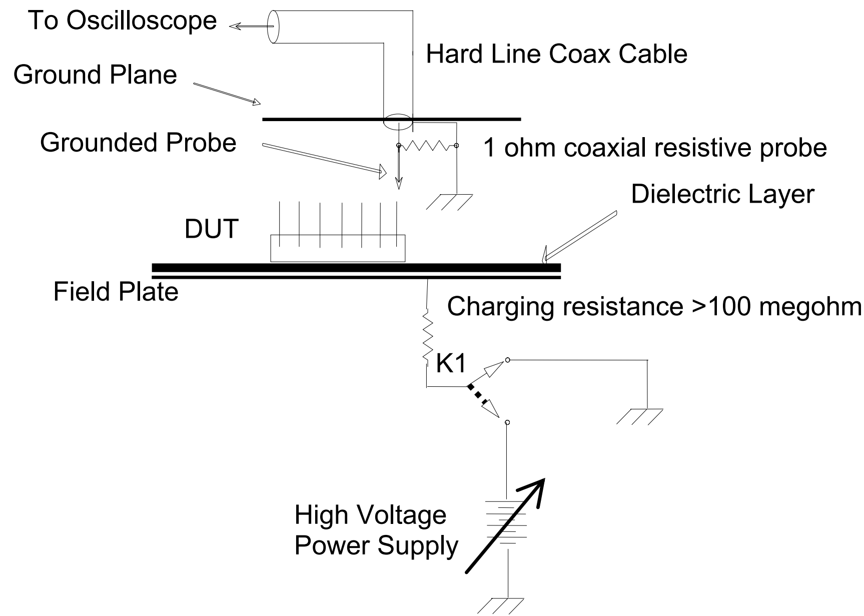

Figure 1: Conceptual Schematic of the CDM Tester

7.2 Waveform Measurement Equipment

7.2.1 Equipment for 3.0 Gigahertz Waveform Measurement

7.2.1.1 Oscilloscope

An oscilloscope or transient digitizer with a real-time (single shot) 3 decibel (dB)-bandwidth (BW) of at least 3.0 gigahertz (GHz) and ≥ 20 gigasample/sec sampling rate with a nominal 50 ohm input impedance.

NOTE: The BW and the sampling rate will affect the observed waveform. Using different oscilloscopes with different BW (rise times) are permitted only if appropriate filtering (software or hardware) is specified to produce a BW and sampling rate equivalent to that specified in Section 7.2.1.1.

7.2.1.2 Attenuator

Attenuator with a precision of 0.1 dB up to 18.0 GHz, a DC precision of the attenuation factor of 5% and an impedance of 50 ± 3 ohms.

7.2.1.3 Probe

A coaxial resistive probe or inductive current transducer with at least five times the BW of the oscilloscope specified (or 18.0 GHz, which ever is less).

7.2.1.4 Cable Assemblies

Cable assemblies with no more than 0.4 dB loss at frequencies up to 18.0 GHz and impedance of 50 ± 2 ohms.

7.2.2 Equipment for 1.0 Gigahertz Waveform Measurement

7.2.2.1 Oscilloscope

An oscilloscope or transient digitizer with a real-time (single shot) 3dB bandwidth (BW) of at least 1.0 GHz with a nominal 50 ohm input impedance. The sampling rate shall be at least five times the BW of the oscilloscope.

NOTE: The user has an option of using a higher BW oscilloscope and using a rise time filter to reduce the rise time to 1.0 GHz. The resulting BW and sampling shall meet that specified in Section 7.2.2.1.

7.2.2.2 Attenuator

Attenuator with a precision of ± 0.1 dB at five times the BW of what is being measured, a DC precision of the attenuation factor of 5% and an impedance of 50 ± 3 ohms.

7.2.2.3 Probe

A coaxial resistive probe or inductive current transducer with at least five times the BW of the oscilloscope being used.

7.2.2.4 Cable Assemblies

Cable assemblies with no more than 0.1 dB loss at frequencies up to five times the BW of the oscilloscope being used and an impedance of 50 ± 2 ohms.

7.2.3 Verification Modules

Two gold-plated or nickel-plated etched copper disks on single-sided insulative circuit board material. Refer to Informative Annex B for information on the verification modules. The circuit board material can be FR-4 or RF-35. Each disk shall be etched in the center of a square of the insulative material. The larger disk shall have a capacitance of 30 pF ± 5%. The smaller disk shall have a capacitance of 4.0 pF ± 5%. The capacitance is measured with the non-metallized (non-disk) side of the verification modules in intimate contact with the metal surface of the grounded FP. The verification module construction is shown in Figures 6 and 7. Specifications for verification modules are presented in Table 5.

NOTE: The module capacitance shall be measured as specified at 1 MHz. If the modules do not comply with the specified capacitance limits, they cannot be used.

NOTE: The FR-4 (abbreviation for Flame Resistant) material is a dielectric (insulative) material made up of epoxy glass, which absorbs moisture. The dielectric constant of this material determines the capacitance of the module. Since the material is known to be sensitive to moisture, this module should be stored in a low moisture environment when not in use. Conditioning or baking may be used to return the module to an acceptable moisture content level. Failure to follow the storage guidelines may result in waveform parameters (e.g. peak currents) that are outside the required specifications. The RF-35 (abbreviation for Radio Frequency) material is not sensitive to moisture and therefore this material does not need to be stored in a low moisture environment.

NOTE: Since both materials (FR-4 and RF-35) have different properties, the user is responsible for the choice of materials.

7.2.4 Capacitance Meter

Capacitance meter with a resolution of 0.2 pF, a measurement accuracy of 3% and a measurement frequency of 1.0 MHz.

7.2.5 Ohmmeter

The ohmmeter used to measure the resistance of the coaxial resistive probe shall be capable of measuring 1.00 ± 0.01 ohms. Use of Kelvin 4-wire connections is advisable.

8.0 PERIODIC EQUIPMENT CALIBRATION, TESTER QUALIFICATION, WAVEFORM RECORDS AND WAVEFORM VERIFICATION REQUIREMENTS

8.1 Equipment Calibration

Calibrate all equipment used for tester or waveform verification in accordance with the manufacturer's recommendations, with a maximum of one year between calibrations. This equipment list includes oscilloscope, attenuator, current transducer, coaxial resistive probe,

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