ASMI Parallel Intel® FPGA IP Core User Guide

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1. ASMI Parallel Intel® FPGA IP Core User Guide

The ASMI Parallel Intel® FPGA IP core provides access to erasable programmable configurable serial (EPCS), quad-serial configuration (EPCQ), low-voltage quad-serial configuration (EPCQ-L), and EPCQ-A serial configuration devices through parallel data input and output ports.

An EPCS device is a serial configuration device that you use to perform an active serial (AS) configuration on supported Intel devices.

An EPCQ/EPCQ-L/EPCQ-A device is a serial or quad-serial configuration that supports AS x1 or AS x4 configuration scheme. During AS configuration, the FPGA device is the master and the EPCS/EPCQ/EPCQ-L device is the slave. For the AS x1 and AS x4 configuration schemes, you must set the MSEL pins for the FPGA devices.

The ASMI Parallel Intel FPGA IP core only supports the EPCS, EPCQ, EPCQ-L, and EPCQ-A devices. If you are using third-party flash devices, refer to the *Generic Serial Flash Interface Intel FPGA IP Core User Guide*.

The ASMI Parallel Intel FPGA IP core implements a basic active serial memory interface (ASMI). To use this IP core, you do not need to know the details of the serial interface and the read and write protocol of an EPCS/EPCQ/EPCQ-L/EPCQ-A device.

The memory in the EPCS/EPCQ/EPCQ-L/EPCQ-A device contains two sections:

- **Configuration memory**—contains the bitstream of the configuration data
- **General purpose memory**—used for an application-specific storage

You can perform the following tasks with the ASMI Parallel Intel FPGA IP core:

- Read the EPCS silicon identification (device identification)
- Protect a certain sector in the EPCS/EPCQ/EPCQ-L/EPCQ-A device from write or erase
- Read the data at a specified address from the EPCS/EPCQ/EPCQ-L/EPCQ-A device
- Perform single-byte write to the EPCS/EPCQ/EPCQ-L/EPCQ-A device
- Perform page write to the EPCS/EPCQ/EPCQ-L/EPCQ-A device
- Read the status of the EPCS/EPCQ/EPCQ-L/EPCQ-A device
- Erase a specified sector on the EPCS/EPCQ/EPCQ-L/EPCQ-A device
- Erase a specified die on the EPCQ-L512 and EPCQ-L1024
- Erase memory in bulk on the EPCS/EPCQ/EPCQ-L256/EPCQ-L512/EPCQ-A device

This figure shows that you can use the ASMI Parallel Intel FPGA IP core to access the general purpose memory portion of the EPCS/EPCQ/EPCQ-L/EPCQ-A devices through the supported FPGA devices.

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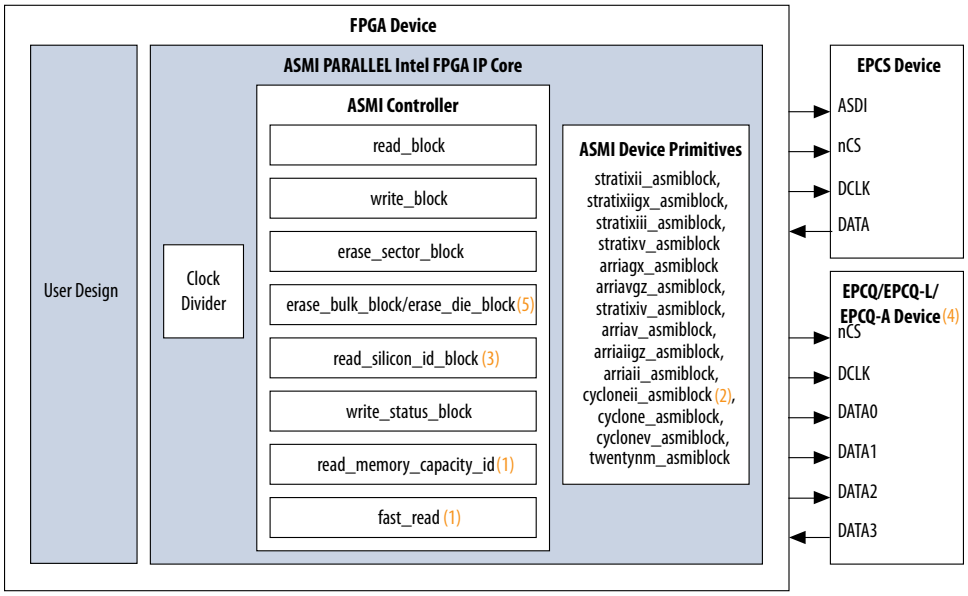
Caution: Intel recommends you to be cautious when accessing the general purpose memory in the configuration devices to avoid corrupting the configuration bits in the configuration memory.

Figure 1. Accessing the General Purpose Memory in the Configuration Devices using the ASMI Parallel Intel FPGA IP Core



(1) Not applicable for EPCS1 and EPCS4.
(2) The synthesis operations for Cyclone III, Cyclone IV GX, Cyclone IV E, and Intel Cyclone 10 LP devices use the cycloneii_asmi primitive.
(3) The read_silicon_id block is supported only for EPCS1, EPCS4, EPCS16 and EPCS64.
(4) Only available for Intel Arria 10 and Intel Cyclone GX devices.
(5) The erase_die_bloack is only available for EPCQ-L512 and EPCQ-L1024 device.

Related Information

- ASMI Parallel Intel FPGA IP Core User Guide Archives on page 33
  Provides a list of user guides for previous versions of the ASMI Parallel Intel FPGA IP core.
- Generic Serial Flash Interface Intel FPGA IP Core User Guide
- Introduction to Intel FPGA IP Cores
  Provides more information about Intel FPGA IP cores.
- Active Serial Configuration
  Provides more information about AS configuration.
- Serial Configuration (EPCS) Devices Datasheet
  Provides more information about EPCS devices.
- Quad-Serial Configuration (EPCQ) Devices Datasheet
  Provides more information about EPCQ devices.
- EPCQ-L Serial Configuration Devices Datasheet
  Provides more information about EPCQ-L devices.
- EPCQ-A Serial Configuration Device Datasheet
  Provides more information about EPCQ-A devices.

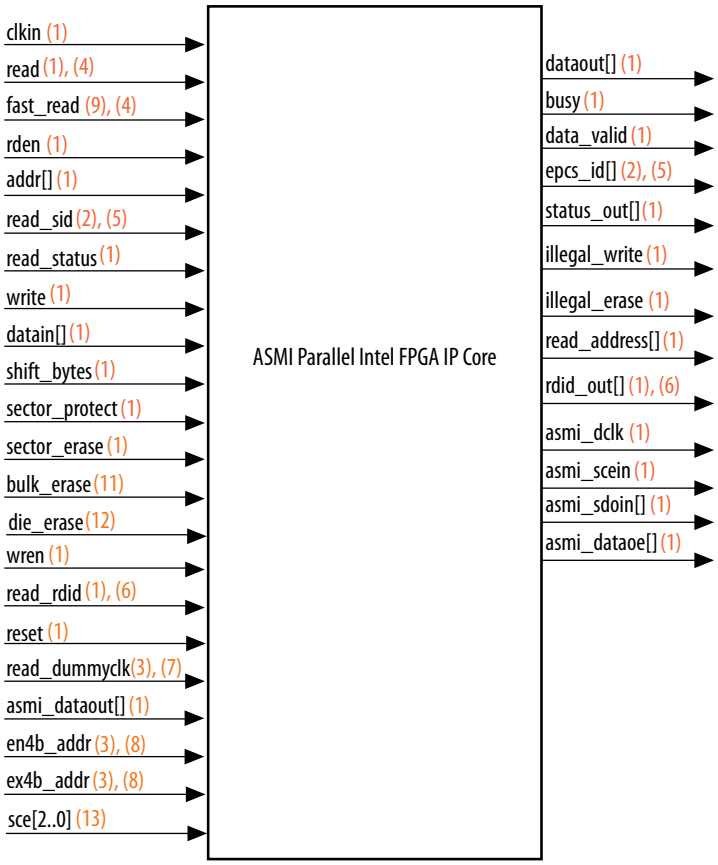
1.1. Device Family Support

The ASMI Parallel Intel FPGA IP core is available for all Intel FPGA device families supported by the Intel Quartus® Prime software except the MAX® series.

1.2. Ports and Parameters

This figure shows a typical block diagram of the ASMI Parallel Intel FPGA IP core.

Figure 2. ASMI Parallel Intel FPGA IP Block Diagram



(1) Applicable for EPCS/EPCQ/EPCQ-L/EPCQ-A devices.
(2) Applicable for EPCS devices only.
(3) Applicable for EPCQ/EPCQ-L/EPCQ-A devices only.
(4) The read and fast_read signals cannot be present simultaneously.
(5) EPCS128 does not support the read_sid and epcs_id signals.
(6) EPCS1 and EPCS4 do not support read_rdid and rdid_out signals.
(7) The read_dummyclk is available only when you select the Use 'fast_read' port option.
(8) The en4b_addr and ex4b_addr signals are supported only for EPCQ256/EPCQ-L256 or larger devices.
(9) Applicable for all EPCS/EPCQ/EPCQ-L/EPCQ-A devices, except for EPCS1 and EPCS4 devices.
(10) Applicable for Intel Arria 10 and Intel Cyclone 10 GX devices only.
(11) Applicable for all EPCS/EPCQ/EPCQ-L/EPCQ-A devices, except for EPCQ512, EPCQ-L512 and EPCQL-1024.
(12) Applicable for EPCQ-L512 and EPCQL-1024 devices.
(13) Applicable for Intel Arria 10 and Intel Cyclone 10 GX devices only.

1.2.1. Parameters

Table 1. Parameter Settings

Parameter	Legal Values	Descriptions
Currently selected device family	Arria GX, Arria II GX, Arria II GZ, Arria® V, Arria V GZ, Cyclone, Cyclone II, Cyclone III, Cyclone III LS, Cyclone IV GX, Cyclone IV E, Cyclone® V, HardCopy III, HardCopy IV, Stratix II, Stratix II GX, Stratix III, Stratix IV, Stratix® V, Intel Arria 10, Intel Cyclone 10 LP, Intel Cyclone 10 GX,	• Specifies the device family you intend to use. Use this parameter for modeling and behavioral simulation purposes, as each device family has its own ASMI primitive.
Configuration device type	EPCS1, EPCS4, EPCS16, EPCS64, EPCS128, EPCQ16, EPCQ32, EPCQ64, EPCQ128, EPCQ256, EPCQ512, EPCQ-L256, EPCQ-L512, EPCQ-L1024, EPCQ4A, EPCQ16A, EPCQ32A, EPCQ64A, EPCQ128A,	• Specify the EPCS/EPCQ/EPCQ-L/EPCQ-A type you want to use. • The default value is EPCS4.
Read Operation		
Use 'read_sid' port	—	• Enables the ability to read the silicon ID of the EPCS device with an active-high `read_sid` input signal. When this signal is asserted, the IP core reads the silicon ID of the EPCS device. After reading the silicon ID, the 8-bit silicon ID appears on the `epcs_id[7..0]`signal until the device resets. • This option is available only for EPCS1, EPCS4, EPCS16, and EPCS64 devices.

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